U.S. ATLAS PROJECT OFFICE

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December 27, 2001

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SUBJECT: U.S. ATLAS Project Monthly Status Report for October 2001

Dear Sirs:

Attached please find Monthly Status Report No. 44 for the U.S. ATLAS Project.

Sincerely yours,

Howard A. Gordon
U.S. ATLAS Deputy Project Manager
Head, U.S. ATLAS Project Office

Distribution:

Abolins, M.
Alam, S.
Baker, K.
Barnett, M.
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Butehorn, C.
Carolan, P. - DOE
Cleland, W.
Crawford, G.
De, K.
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Firestone, A. - NSF
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Hinchliffe, I.
Huth, J.
Kagan, H.
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Slattery, P.
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Tuts, M. – PAP
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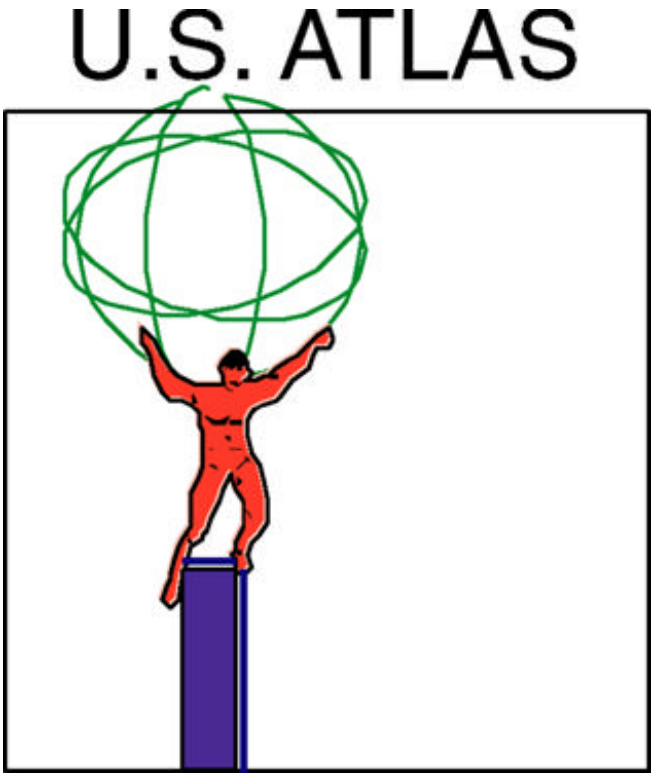
Wu, S.L.
Yeck, J.



PROJECT STATUS REPORT NO. 44

REPORTING PERIOD

OCTOBER 2001

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1. PROJECT OBJECTIVE

The U.S. ATLAS Project consists of the activities to design, supply, install and commission the U.S. portion of the ATLAS detector. The detector will become part of the Large Hadron Collider (LHC) at CERN, the European Laboratory for Particle Physics. The ATLAS detector is being designed to understand the dynamics of electroweak symmetry breaking. The U.S. ATLAS collaboration is funded jointly by the U.S. Department of Energy and the National Science Foundation.

The fundamental unanswered problem of elementary particle physics relates to the understanding of the mechanism that generates the masses of the W and Z gauge bosons and of quarks and leptons. To attack this problem, one requires an experiment that can produce a large rate of particle collisions of very high energy. The LHC will collide protons against protons every 25 ns with a center-of-mass energy of 14 TeV and a design luminosity of 10^{34} cm^{-2} s^{-1}. It will probably require a few years after turn-on to reach the full design luminosity.

The detector will have to be capable of reconstructing the interesting final states. It must be designed to fully utilize the high luminosity so that detailed studies of rare phenomena can be carried out. While the primary goal of the experiment is to determine the mechanism of electroweak symmetry breaking via the detection of Higgs bosons, supersymmetric particles or structure in the WW scattering amplitude, the new energy regime will also offer the opportunity to probe for quark substructure or discover new exotic particles. The detector must be sufficiently versatile to detect and identify the final state products of these processes. In particular, it must be capable of reconstructing the momenta and directions of quarks (hadronic jets, tagged by their flavors where possible), electrons, muons, taus, and photons, and be sensitive to energy carried off by weakly interacting particles such as neutrinos that cannot be directly detected. The ATLAS detector will have all of these capabilities.

The ATLAS detector is expected to operate for twenty or more years at the CERN LHC, observing collisions of protons, and recording more than 10^7 events per year. The critical objectives to achieve these goals are:

- Excellent photon and electron identification capability, as well as energy and directional resolution.
- Efficient charged particle track reconstruction and good momentum resolution.
- Excellent muon identification capability and momentum resolution.
- Well-understood trigger system to go from 1 GHz raw interaction rate to ~100 Hz readout rate without loss of interesting signals.
- Hermetic calorimetry coverage to allow accurate measurement of direction and magnitude of energy flow, and excellent reconstruction of missing transverse momentum.
- Efficient tagging of b-decays and b-jets.

The U.S. ATLAS cost objective is $163.75M while supplying initially the work scope described in Appendix 3 of the Project Management Plan (PMP) and, if possible, all the goals described in Appendix 2 of the PMP.

The ATLAS project was initiated in FY 1996, and is scheduled for a 10-year design and fabrication period beginning in the first quarter of FY 1996, and finishing in FY 2005. This period will be followed by operation at the LHC.

2. TECHNICAL APPROACH CHANGES

No change.

3. PROJECT MANAGER'S SUMMARY ASSESSMENT – W. Willis

The U.S. ATLAS Construction Project has moved into the phase where most of the deliverables are in production. This leads to a rapid increase in Earned Value and consequently in fractional Contingency. This simple model flies in the face of the reality that unforeseen difficulties must occur at some probability. In this month, both effects can be seen in the report. Great progress has been achieved in producing the detectors for ATLAS. A few problems have emerged which will surely lead to claims against Contingency. The most evident is the discovery that the baseline gas used in the straw tubes of the Transition Radiation Tracker, containing some CF_4, destroys the glass wire joints under heavy exposure to charged tracks. This effect may depend on the detailed environment, such as the moisture level, so as to have escaped previous tests, but this susceptibility gives rise to very serious concern, and is occupying the first priority of the group. The two most likely options are to replace the gas with one less aggressive, or to replace the type of wire joint. If the former is chosen, there will be a performance penalty that may be evaluated as small, in the latter case, many tubes will have to be re-strung, at a substantial cost and delay. No doubt the unpleasant consequences will lead to a serious look at the value of the performance gained from the use of this unconventional gas.

In other cases, small differences from the original specifications are dealt with work-arounds. For example in the case of the readout for Silicon Strips, WBS 1.1.2, the current drawn by the ABCD readout chip after heavy irradiation is somewhat above the original specification. The cause of this effect has been understood, but it has been found to be more advantageous to increase the current rating of the power supplies than to reopen the layout of the chips. We may hope that the surprises we encounter as we continue production are at the level of these examples, which will not require a very large use of our Contingency.

4. TECHNICAL PROGRESS - SUBSYSTEM MANGERS' SUMMARIES

1.1 Subsystem Manager's Summary — Abe Seiden (University Of Calif. At Santa Cruz)

1.1.1 Pixels

The layout and verification of the pixel readout chip has been completed and the chip files forwarded for fabrication. Considerable care has been taken with the layout and completeness of this chip to minimize the number of iterations required in the future. The first set of wafers with chips are due back in the middle of January.

The sensor design and qualification is pretty complete. The group is ready to place the first orders for pixel silicon sensors. A BCP to allow purchase of the sensors has now been submitted.

The various parts of the mechanics that support the pixel disks are rather complete and the group remain on schedule for the global support frame PRR in February 2002. The more extended mechanics which support the pixel system, support the beam tube, and interface to the SCT are under design. Funds for the beam pipe support effort are not currently available but urgently needed. An area of concern is the end region of the support tube where the interfacing to the many services (electrical, cooling, optical components) via patch panels is a difficult issue given the density of items coming together.

Work on the flex hybrids and opto-readout continue with new iterations to be tested over the next few months.

1.1.2

The second batch of ABCD wafers has been delivered with ATMEL remaining on their accelerated schedule. The new epi vendor has now been qualified and future deliveries of chips with the new epi are expected next month. Testing is continuing with changes to the test program to reduce the time taken to test a wafer being looked at slowly to make sure this does not introduce changes in the yield or test criteria.

The module and hybrid construction efforts are moving ahead expeditiously. Various fixtures are being made and several modules have been constructed to test and optimize procedures. A short-term plan to move hybrid production and test forward has been developed. The goal is to start hybrid production in January. Work on fixtures and procedures to remove and replace defective chips are being developed.

1.1.3

The prototype ROD continues to be exercised with small software errors found and fixed. This is an extensive and exhaustive procedure since the boards are very complex. The 15 boards to be used in more extensive system testing are in fabrication and parts are ready for loading. These cards will form the basis of the several month user evaluations to begin in early 2002. The user evaluation is now expected to last into April 2002 with a final design review about a month later. The pixel ROD design review is approximately on the same timetable.

1.2 Subsystem Manager's Summary **Harold Ogren (Indiana University)**

Component production at Hampton has increased this month, and module production continues at both Duke and Indiana University, although a number of concerns about alignment (at Duke) and leak testing (at Indiana) have slowed module production from the rates we obtained last month.

A much more serious problem with the robustness of the glass wire joints surfaced this month. Duke had constructed a testing fixture of 24 straws using the operational gas of Xe- CF_4- CO_2. Using a Duke bank of large Sr sources, the potential wire aging (loss of gain) at LHC rates and higher could be studied. The expressed focus being the effect the glass wire joint might have on wire aging. It was expected that the test would run several months. However, after only two weeks a wire joint broke. Examination of the wire showed that the glass joints had been seriously degraded. This result has also been confirmed using Ar- CF_4- CO_2 at Indiana.

We are now in the process of understanding this effect. We have instituted several follow up measurements, started a search for alternate wire joints, and begun the study of a binary gas (without CF_4). Until we have resolved the problem and decided on the solution, we have stopped wire joint production at Duke, and halted wire stringing at both assembly sites—Duke and Indiana. We will attempt to accelerate mechanical production using the spare assembly personnel during the pause in wire stringing.

Electronics - 1.2.5

A few further tests on the ASDBLR00 noise performance confirm our initial impression that the increased noise is due to an error in estimating (extracting) the capacitance associated with the input protection network. ATMEL has finished processing the new wafers (we will get seven) and we received them in early Nov. Those devices should be back by the third week in November at which point we get to learn which of the variations in input protection is optimal in terms of noise/protection trade off. Unless there are further surprises that should allow us to freeze the ASDBLR design and prepare for a design review (PRR) in early 2002 (probably end of January or mid February 2002.

All DTMROC design effort is concentrated on the DSM version. We believe that all blocks are complete and verified, that the tools exist to verify the complete design, and that we are ready for a final design review. This review has been scheduled for Nov. 15. At the last TRT meeting in CERN in Oct. it was proposed that we add in temperature and voltage measurement capability to the design - this opens the possibility of reducing the services cable plant in the ID and giving us much finer grained monitoring of the operating environment. The extra circuitry required is minimal and the only new cells (a precision comparator and a diode) have already been designed and verified.

We have made some progress on Barrel testing, have mapped out the response of the flex boards along a snake cable and, at the digital level, demonstrated good performance—the snake cable seems to work well as a data transmission medium—we have worked extensively with Lund in developing the design for a non-flex FBGA based three (or two) layer postage stamp design. This design is now well advanced and should be available as a completed printed circuit prior to delivery of actual FBGA devices.

1.3 Subsystem Manager's Summary Richard Stroynowski (Southern Methodist University)

Steady progress on all fronts: the production of all electronics components, FCAL and system crates is proceeding well. The two outstanding items are:

1) Production and installation of feedthroughs (FT) is proceeding very well. The completion of the installation of all FTs on the barrel appears to be on, and even ahead of schedule.

2) The prototype Front End Board (FEB) has been finalized. All custom ASIC chips appear to be working well. The decision has been made to proceed with the cheaper DSM technology for the SCA Controller. This technology will also be used for Gain Selector and Clock Distribution chips. Prototypes of one type of voltage regulators exist and undergo testing at CERN.

1.4 Subsystem Manager's Summary Lawrence Price (Argonne National Lab.)

Submodule production is close to finished, except for a few more months of fixes and special cases. By the end of October, the University Of Illinois had only 8 submodules remaining to be shipped, 5 of which were already stacked. The University of Chicago completed its complement of submodules earlier. 44 of 65 modules have been built and 36 have been instrumented, tested, and shipped to CERN. There was one anomalous situation with module assembly in October, when it was discovered that the endplate was not aligned correctly. Correction is expected to be reasonably straightforward. In the structural analysis work, seismic loads were added to the model, and a complete 3D solid model of the EB saddles was started. Instrumentation is proceeding well. The state of the art is indicated in the production during the month of the best (lowest rms light variation) module so far (40) and the worst for some time (38). Continued attention and care is clearly important. The final batch of tiles have been shipped from CERN and is expected to be distributed to MSU in November. Work continued at Illinois on the STEP2 (pulsed) PMT testing. This has been a hard job and the system is not completely operational yet. 84% of the 3-in-1 cards have been tested and shipped to CERN. Some faulty cards have been set aside for later repairs. All motherboard segments and mezzanine cards have been received at Chicago and burn-in and testing is underway. 12% have been shipped.

1.5 Subsystem Manager's Summary Frank Taylor (MIT)

The MDT Series II chamber production continued on schedule. At the end of October 2001 roughly 30% of the 240 required base chambers were made. Drawings of chambers, tooling and chamber services for Series III were worked on at Brandeis, Harvard and Washington. Design and testing of components of the MDT electronics continued. Work at the CSC production site at BNL continued to be focused on setup and production development of cathode panels. System integration and Parameter Book updating took place at Brandeis.

Most MD tube parts remain off the critical path except for endplugs where both Michigan and Seattle ran out of the standard 'NIEF' type. This problem was anticipated but unfortunately our remediation using a second source of endplugs from a German outfit was only partially successful due to the low quality of these endplugs. The vendor has been notified and ATLAS management, who proposed to use the same vendor, has been informed.

MDT base-chamber production is ahead of schedule at Michigan and Seattle and on schedule at BMC. Both Michigan and Seattle are installing Faraday cages and gas systems on a production basis. At the

BMC, tooling for the tubelet installation was under development. Michigan anticipates completion of their Series II chamber production by Jan. '02 and Seattle by Dec. '01. The BMC, who are making a 4 layer chamber series, anticipates completion of their Series II by March '02.

On the MDT electronics front, the ASD prototypes have been successfully bench tested. Checks are being made to verify that the achieved parameters are acceptable. Production of the HV hedgehog distribution card is expected in early '02 - although the chamber makers could certainly use the HV and signal boards now.

CSC cathode panel fabrication will take place at BNL. Acceptable samples have been made and vendors lined up and parts procurement underway. A production plan has been developed. The CSC off-chamber electronics work at UCI continued with programming of the Sparsifier among other things. An internal review of the CSC status took place Nov. 14 at BNL.

Alignment parts fabrication continued at Brandeis ahead of chamber fabrication need. Integration design and testing of components for the H8 test facility at CERN continued.

1.6 Subsystem Manager's Summary **Robert Blair (Argonne National Lab.)**

Work on the current software framework for phase 2 is continuing. Architectures for phase 2 tests were discussed during ATLAS week and a simple system of concentrating switches and one or two central switches was arrived at as the "strawman" for implementation. A modest system size is considered adequate initially. Production of a prototype supervisor RoI builder (SRB) has been postponed. This will allow for a more rigorous design process, more in line with the production of final level 1 components. The delay will not significantly impact progress in other areas.

1.10 Technical Coordination **David Lissauer (Brookhaven National Laboratory)**

LAr HEC/Forward Review:
A system review of the LAr Forward and Hadronic system took place. An action list is being developed as a result of the review. In general, these two systems are in reasonable shape.

Magnet Review:
A system review of the Barrel Magnet system took place. The review was useful. The Barrel system has made significant progress in the last year. Most of the contracts are out, and the main open issues have to do with the installation plan. There are quite a few interface questions still to be resolved in the next three months. The EC Toroid has some serious production problems. The cold mass assembly, a NIKEFF responsibility awarded to a Dutch company, is behind schedule. The company has been taken over and the new owners are not willing to lose money on this contract. Discussions are on-going but it is not clear if a new contract with a different company will have to be pursued or if the present company will be able to complete the job. This means a very significant delay and significant cost increases in this project. (The cost increase is not clear yet but is in the order of millions of CHF).

U.S. Review of U.S. Effort in Technical Coordination:
A U.S. review of Technical Coordination activities took place. While the main purpose was to review U.S. contributions, it was not possible to do that without taking a look at the overall TC activities. While there was a lot of progress in TC during the last nine months since M. Nessi took over, it is clear that not all

problems have been solved. The U.S. contributions were judged to be significant and should continue. The exact levels are to be determined by ATLAS needs and priorities.

Technical Coordination Meetings:
During the week a number of meetings were held to discuss work progress as it relates to Technical Coordination. One of the main efforts at present is to organize working groups that will be looking into the installation, survey and placement requirements of the different detectors. We have by now organized four working groups to look into the feet, Barrel Toroid installation, Calorimeter installation (both Barrel and endcap) and the inner detector installation.

Activity A Meeting:
A meeting of the Activity A task leaders took place. We discussed some of the feedback from the US review of Technical Coordination. The final report has not been issued yet – but the feedback has been positive. The agenda for the Magnet review in December has been agreed upon, and people are starting to work with the Muon system to understand the schedule, resources, safety questions etc.

5. OPEN ITEMS BETWEEN DOE/NSF AND U.S. ATLAS

a) Financial: There is $292,000 of available funding residing in management reserve, $5,150,000 available in management contingency and $17,892,000 of undistributed budget authority, pending completion and approvals of FY 02 Institutional MOU's. Table 7-2 contains the summary of FY02 funds distribution. There was $4,036,300 requested in additional funding allocations during October.

b) Schedule: None.

c) Technical: None.

6. SUMMARY ASSESSMENT AND FORECAST

1. Financial Status

A total of $119,445,000 (72.9%) was authorized, held in reserve or identified as undistributed budget of the $163.75M Total Project Cost Objective. The details of the overall project cost objective are presented in Table 6-1 reproduced overleaf from the U.S. ATLAS Project Plan as approved on 3/18/98 and revised to include cost changes approved through BCP # 49.

The details of the reported costs and reported obligations are presented in the Table 7-1 in Section 7 of this report. In addition Table7-2 shows the fiscal year 2002 funding allocation by institution and funding source.

The relationship between budget authority/cost/obligations (including an estimate of other accrued costs and obligations) is presented in Figure 9-1 in Section 9 of this report.

The level 2 CSSR statistics are presented in section 10. Performance analysis is included for major subsystems in section 8 of this report.

2. Schedule Status

See details in Figure 11-1.

The overall schedule status report is found in section 11.

The milestone log from the PMP, including revised forecast dates, is reproduced as section 12.

3. Baseline Change Proposals

Forty-nine BCPs were received through October 2001. Forty-seven BCP's were approved and two were withdrawn.

Table 6-1 reflects cost changes through BCP # 49.

TABLE 6-1: SUMMARY COST ESTIMATE

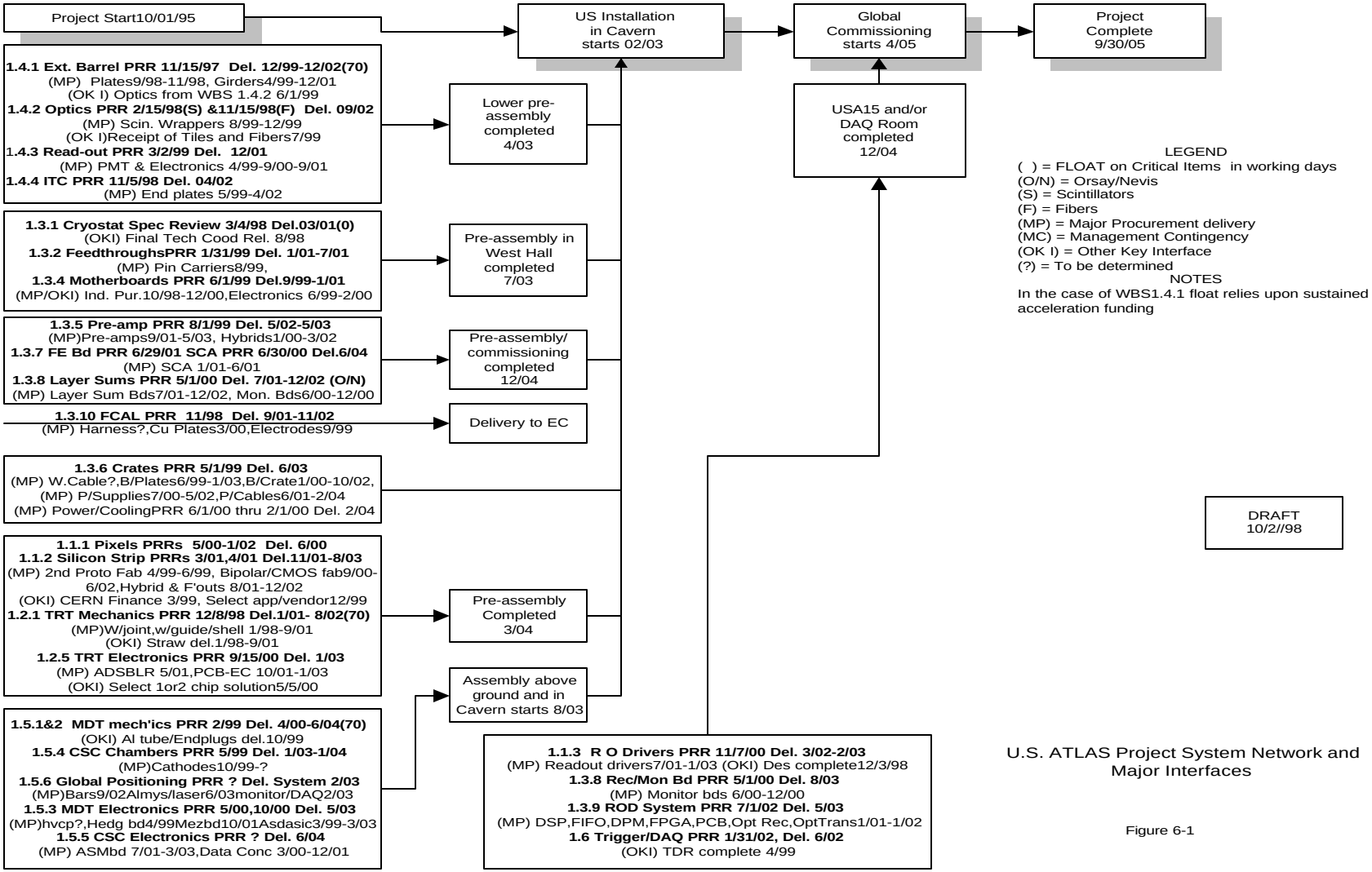
U.S.ATLAS Project
Summary Cost Estimate

Presented in (AY$ x 1000)

WBS No.	Description	Base Cost
	Technical Baseline	
1	U.S. ATLAS	
1.1	Silicon	17,795.3
1.2	TRT	9,194.0
1.3	LAr Calorimeter	43,771.7
1.4	Tile Calorimeter	9,290.2
1.5	Muon Spectrometer	26,391.2
1.7	Common Projects	9,179.1
1.8	Education	286.5
1.9	Project Management	8,279.0
1.10	Technical Coordination	450.0
	Subtotal	**124,637.0**
1.6	Trigger/DAQ Pre-Technical Baseline	3,117.9
	Subtotal	**3,117.9**
	Management Contingency	**8,709.7**
	Contingency	**19,446.0**
	Subtotal	**28,155.6**
	Technical Baseline	**155,910.5**
Items Outside of Approved Technical Baseline		
1.1.1	Pixels	-
1.6	Trigger/DAQ	**7,839.5**
	Subtotal	**7,839.5**
	Total Project Cost**	**163,750.0**

** Assumes funding profile of FY96=$1.7M, FY97=$3.7M, FY98=$10.05M,, FY99=$25.63 FY00=$28.4M, FY01=$26.8M, FY02=$23.2M, FY03=$24.7M,FY04=$14.7M, FY05=$4.9M.
project completion in 2005.
Includes cost changes for BCP 1-49.

Figure 6-1 - Project System Network



U.S. ATLAS Project System Network and Major Interfaces

Figure 6-1

FUNDING

Table 7.1 - Summary of Funds Authorized & Total Costs and Commitments to Date

U.S. ATLAS Project
Summary of Funds Authorized
and
Total Costs and Commitments to Date
October 31, 2001
(AY$ x 1,000)

WBS No.	Description	Funds Authorized Thru FY02	Expenses + Commitments			Balance of Authorized Funds
			Expenses to Date	Open Commit	Total to Date	
1.1	Silicon	13,598	9,789	60	9,849	3,749
1.2	TRT	7,473	5,528	683	6,211	1,262
1.3	LAr Calorimeter	31,964	23,441	3,239	26,680	5,285
1.4	Tile Calorimeter	9,175	7,857	19	7,876	1,299
1.5	Muon Spectrometer	17,673	14,099	98	14,197	3,477
1.6	Trigger/DAQ	2,310	1,725	5	1,730	580
1.7	Common Projects	7,269	7,132	-	7,132	137
1.8	Education	49	47	-	47	2
1.9	Project Management	6,150	4,767	17	4,784	1,366
1.10	Technical Coordination	450	293		293	157
	Subtotal	96,111	74,678	4,120	78,798	17,313
	Management Reserve	292			-	292
	Contingency	5,150			-	5,150
	Subtotal	101,553	74,678	4,120	78,798	22,755
	Undistributed Budget	17,892			-	17,892
1	U.S. ATLAS Total AY$	119,445	74,678	4,120	78,798	40,647

Table 7.2 – FY01 Funds – U.S. ATLAS Summary by Institution and Subsystem

U.S. ATLAS
FY 02 Funds
WBS 1 U.S. ATLAS Summary
Presented in (AY$x1,000)
Status as of 10/31/01

	WBS 1.1 Silicon			WBS 1.2 TRT			WBS 1.3 Liquid Argon			WBS 1.4 Tile			WBS 1.5 Muon			WBS 1.6 Trigger/DAQ			WBS 1.7 Common Projects			WBS 1.8 Education		WBS 1.9 Proj Mgmt			WBS 1.10 Tech Coord			WBS 1 U.S. ATLAS Total FY01			
	DOE		NSF	DOE		NSF	DOE		NSF	DOE		NSF	DOE		NSF	DOE		NSF	DOE		NSF	DOE	NSF	DOE		NSF	DOE		NSF	DOE		NSF	
Institution	Grant	Contract		Grant	Contract		Grant	Contract		Grant	Contract		Grant	Contract		Grant	Contract		Grant	Contract				Grant	Contract		Grant	Contract		Grant	Contract		Total
ANL											166						233													391			391
BNL								1,000						445											700					2,145			2,145
LBNL		1,500																												1,500			1,500
SUNY/Albany																																	-
Arizona																																	-
Boston University																																	-
Brandeis University																																	-
UC Irvine																																	-
UC Santa Cruz																																	-
U of Chicago																																	-
Duke University																																	-
Hampton University																																	-
Harvard University																																	-
U of Illinois																																	-
Indiana University																																	-
MIT																																	-
Michigan State U																																	-
Nevis/Columbia																																	-
New Mexico																																	-
North Illinois U																																	-
Ohio State University																																	-
U of Michigan																																	-
U of Oklahoma *																																	-
U of Pennsylvania																																	-
U of Pittsburg																																	-
U of Rochester																																	-
UT- Arlington																																	-
Southern Methodist U																																	-
SUNY/Stony Brook																																	-
Tufts University																																	-
U of Washington																																	-
U of Wisconsin																																	-
Total FY01	-	1,500	-	-	-	-	-	1,000	-	-	166	-	-	445	-	-	233	-	-	-	-	-	-	700	-	-	-	-	-	4,036	-	-	4,036
Reserve																	-			-				-	-		-			-			-
Contingency																								-	-		-			-			-
Total FY01	-	1,500	-	-	-	-	-	1,000	-	-	166	-	-	445	-	-	233	-	-	-	-	-	-	700	-	-	-	-	-	4,036	-	-	4,036

* correction of prior month record of 426 to 49

8. PERFORMANCE ANALYSIS

Status through the month of October 2001 reflects the new baseline schedules for all subsystems. The re-baseline date was established on October 1, 2000 and the Estimate to Complete 01 (ETC 01) was defined as all tasks and resources required to complete the project. All prior efforts were equated to the actual costs expended. The schedules are resource loaded to the baseline funding of $163,750K with Contingency, Management Contingency, and Items Outside of the Approved Baseline shown on separate lines and excludes all NSF R&D funds.

The CSSR in section 10 shows $79,406.5k of the work has been performed, which represents approximately 62.2% of the work authorized to date. There is an unfavorable schedule variance of ($1,697.8k) or 2.1% behind the plan. There is a favorable cost variance of $4,728.9k or 6.0% under spent for the work accomplished. This jump in the favorable cost variance is the result of the basic planning approach where material dollars are lumped in planning packages at the end of the fiscal year, then, when orders are placed these dollars are moved to the period when material payments will be made. In situations where tasks are behind schedule the money or material costs were lower than planned this left over money adds to a positive cost variance. There are outstanding commitments of $4,120.4k at this time that do not show up in the performance. This analysis will provide a breakdown of these variances into the individual subsystems and identify the specific tasks that cause these variances.

WBS 1.1 SILICON

Summary
The CSSR shows that $10,569.1k of the work has been completed which represents 59.4% of the total effort for the Silicon subsystem. There is an unfavorable schedule variance of ($354.8k) or 3.2% behind the plan and a favorable cost variance of $780.3k or 7.4% under spent for the work accomplished. There are outstanding commitments of $59.9k at this time that do not show up in the performance.

Schedule Variance
The unfavorable schedule variance is concentrated in the following WBS level 3 elements:

WBS 1.1.3 RODs SV = ($284.0k)

- Design ROD Cards is behind plan ($6.1k)
- ROD Test Stand is behind plan ($21.3k)
- ROD Prototypes is behind plan ($25.6k)
- ROD Prototype Evaluation is behind plan ($40.4k)
- ROD Production Model is behind plan ($81.7k)
- ROD Fabrication is behind plan ($108.8k)

Cost Variance
There is a favorable cost variance of $780.3k which is distributed as follows: Pixel $196.62k, the Silicon Strip System $756.3k and the ROD Design and Fabrication ($172.5k).

WBS 1.2 TRT

Summary
The CSSR shows that $6,447.1k of the work has been completed which represents 70.1% of the total effort for the TRT subsystem. There is an unfavorable schedule variance of ($462.1k) or 6.7% behind the

plan and a favorable cost variance of $918.7k or 14.2% under spent for the work accomplished. There are outstanding commitments of $682.9k at this time that do not show up in the performance.

Schedule Variance
The unfavorable schedule variance is concentrated in the following WBS level 3 elements

WBS 1.2.1 Barrel Mechanics SV = ($461.0k)

- Detector Elements are behind plan ($243.8k)
- Component Assembly is behind plan ($78.2k)
- Module Assembly #2 (Duke) is behind plan ($78.2k
- Module Assembly #1 (IU) is behind plan ($59.8k)
-

Cost Variance
There is a favorable cost variance of $918.7k that is distributed as follows: Barrel Mechanics $662.4k and TRT Electronics $256.3k.

WBS 1.3 LAr

Summary
The CSSR shows that $25,724.4k of the work has been completed which represents 58.8% of the total effort for the LAr subsystem. There is an unfavorable schedule variance of ($590.4k) or 2.2% behind the plan and a favorable cost variance of $2,283.9k or 8.9% under spent for the work accomplished. There are outstanding commitments of $3,239.0k at this time that do not show up in the performance.

Schedule Variance
The unfavorable schedule variance is concentrated in the following WBS level 3 elements:

WBS 1.3.1 Barrel Cryostat SV = ($154.7k)
WBS 1.3.2 Feedthroughs SV = ($98.4k)
WBS 1.3.7 Front End Board SV = ($169.4k)
WBS 1.3.10 Forward Calorimeter SV = ($81.6k)

Cost Variance
The favorable cost variance of $2,283.9k is a combination of positive and negative variances concentrated in the following WBS Level 3 elements.

- 131 Barrel Cryostat CV = $307.9k
- 132 Feedthroughs CV = ($172.1k)
- 133 Cryogenics CV = $636.7k
- 134 Readout Electrodes/MB CV = $434.1k
- 135 Preamp/Calibration CV = $278.3k
- 136 System Crate Integration CV = $465.2k
- 137 Front End Board CV = ($153.0k)
- 139 ROD System CV = $145.6k
- 1310 Forward Calorimeter CV = $230.6k

WBS 1.4 TILE

Summary
The CSSR shows that $8,564.2k of the work has been completed which represents 92.2% of the total effort for the Tile subsystem. There is an unfavorable schedule variance of ($51.1k) or 0.6% behind the plan and a favorable cost variance of $707.2k or 8.3% under spent for the work accomplished. There are outstanding commitments of $19.1k at this time that do not show up in the performance.

Schedule Variance
The unfavorable schedule variance is concentrated in the following WBS level 3 elements:

WBS 1.4.4 Intermediate Tile Calorimeter SV = ($48.4k)

- Scintillator Preparation is behind plan ($17.4k)
- Cryostat Scintillators are behind plan ($26.2k)

Cost Variance
There is a favorable cost variance of $707.2k which is distributed as follows:

- 141 EB Mechanics $28.0k
- 142 EB Optics ($51.9k)
- 143 Readout $214.9k
- 144 ITC $516.1k

WBS 1.5 MUON

Summary
The CSSR shows that $14,011.8k of the work has been completed which represents 53.1% of the total effort for the Muon subsystem. There is an unfavorable schedule variance of ($154.6k) or 1.1% behind the plan and an unfavorable cost variance of ($87.2k) or 0.6% over spent for the work accomplished. There are outstanding commitments of $97.5k at this time that do not show up in the performance.

Schedule Variance
The unfavorable schedule variance is concentrated in the following WBS level 3 elements:

WBS 1.5.7 MDT Chambers SV = ($46.7k)

- Special Chamber Integration Drawings ($16.3k)
- Common Procurements ($9.9k)
- Chamber Construction ($20.2k)

WBS 1.5.8 MDT Supports SV = ($81.9k)

- Chamber Mount Struts Design is behind plan ($28.8k)
- Integration with Support Structure Design is behind plan ($36.5k)
- Chamber Mount Struts are behind plan ($12.9k)

Cost Variance
The unfavorable cost variance of $87.2k is a combination of positive and negative variances concentrated in the following WBS Level 3 elements.

- 154 CSC Chambers CV = $116.9k

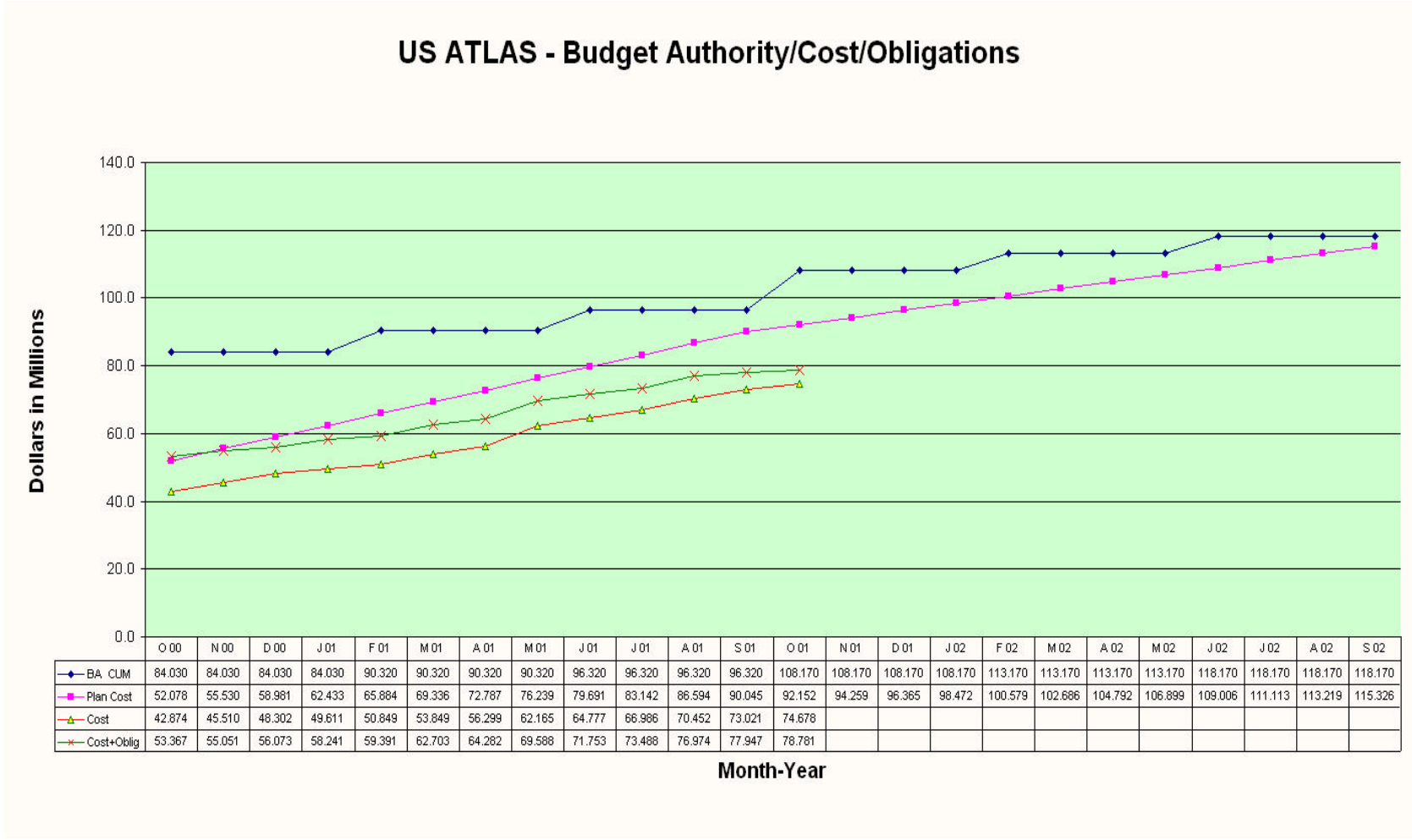
- 157 MDT Chambers CV = ($110.5k)
- 158 MDT Supports CV = ($98.0k)
- 159 MDT Electronics CV = $403.8k
- 1511 CSC Electronics CV = ($144.3k)
- 1512 Global Align System CV = ($255.20k)

WBS 1.6 TRIGGER/DAQ

Summary

The CSSR shows that $1,851.4k of the work has been completed which represents 59.4% of the total effort for the Trigger/DAQ subsystem. There is an unfavorable schedule variance of ($84.7k) or 4.4% behind the plan and a favorable cost variance of $126.1k or 6.8% under spent for the work accomplished. There are unfavorable cost variances of ($93.9k) for the Level 2 Supervisor and ($0.9k) for Architecture, but, these are offset by favorable cost variances of $146.0k.8k for the Level 2 Calorimeter Trigger and $74.9k for the Level 2 SCT Trigger. There are outstanding commitments of $4.6k at this time that do not show up in the performance.

9. BUDGET AUTHORITY COSTS AND OBLIGATIONS



	O 00	N 00	D 00	J 01	F 01	M 01	A 01	M 01	J 01	J 01	A 01	S 01	O 01	N 01	D 01	J 02	F 02	M 02	A 02	M 02	J 02	J 02	A 02	S 02
BA_CUM	84.030	84.030	84.030	84.030	90.320	90.320	90.320	90.320	96.320	96.320	96.320	96.320	108.170	108.170	108.170	108.170	113.170	113.170	113.170	113.170	118.170	118.170	118.170	118.170
Plan Cost	52.078	55.530	58.981	62.433	65.884	69.336	72.787	76.239	79.691	83.142	86.594	90.045	92.152	94.259	96.365	98.472	100.579	102.686	104.792	106.899	109.006	111.113	113.219	115.326
Cost	42.874	45.510	48.302	49.611	50.849	53.849	56.299	62.165	64.777	66.986	70.452	73.021	74.678											
Cost+Oblig	53.367	55.051	56.073	58.241	59.391	62.703	64.282	69.588	71.753	73.488	76.974	77.947	78.781											

10. WBS – COST SCHEDULE STATUS REPORT

Project Status Report
Section 10

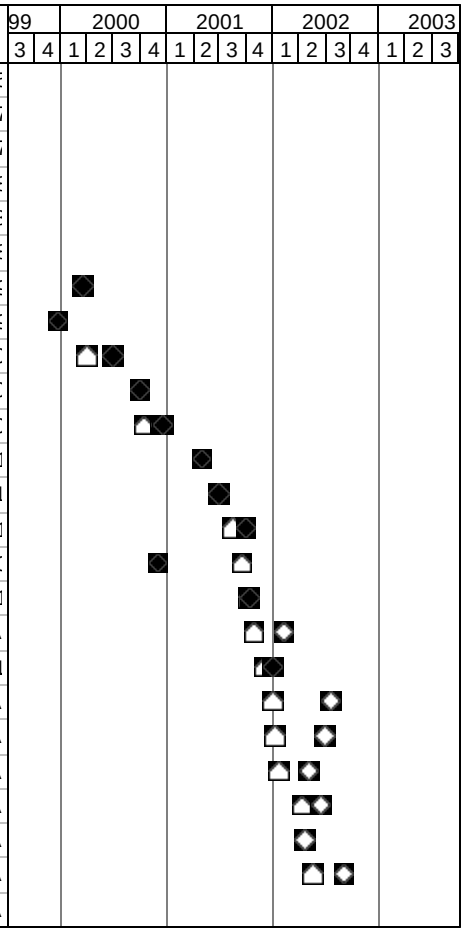
U.S. ATLAS
Cost Schedule Status Report
Reporting Period Ending:10/31/01

		Cumulative To Date (k$)					At Completion (k$)			Complete (%)		
		Budgeted Cost		Actual Cost	Variance			Latest				
	WBS Element	Work Scheduled	Work Performed	Of Work Performed	Schedule	Cost	Budgeted AY $s	Revised Estimate	Variance	Scheduled	Performed	Actual
1.1	Silicon	10,923.9	10,569.1	9,788.8	(354.8)	780.3	17,795.3	17,795.3	-	61.4	59.4	55.0
1.2	TRT	6,909.2	6,447.1	5,528.4	(462.1)	918.7	9,194.0	9,194.0	-	75.1	70.1	60.1
1.3	Liquid Argon	26,314.8	25,724.4	23,440.5	(590.4)	2,283.9	43,771.7	43,771.7	-	60.1	58.8	53.6
1.4	TileCal	8,615.2	8,564.2	7,857.0	(51.1)	707.2	9,290.2	9,290.2	-	92.7	92.2	84.6
1.5	Muon	14,166.4	14,011.8	14,099.0	(154.6)	(87.2)	26,391.2	26,391.2	-	53.7	53.1	53.4
1.6	Trigger/DAQ	1,936.2	1,851.4	1,725.4	(84.7)	126.1	3,117.9	3,117.9	-	62.1	59.4	55.3
1.7	Common Projects [1]	7,132.2	7,132.2	7,132.2	-	-	9,179.1	9,179.1	-	77.7	77.7	77.7
1.8	Education [1]	47.2	47.2	47.2	-	-	286.5	286.5	-	16.5	16.5	16.5
1.9	Project Management [1]	4,766.6	4,766.6	4,766.6	-	-	8,279.0	8,279.0	-	57.6	57.6	57.6
1.10	Technical Coordination	292.6	292.6	292.6	-	-	450.0	450.0	-	65.0	65.0	65.0
Sub Total		81,104.3	79,406.5	74,677.7	(1,697.8)	4,728.9	127,754.9	127,754.9	-	63.5	62.2	58.5
Management Reserve							0.0	0.0	-			
Contingency							19,446.0	19,446.0	-			
Management Contingency							8,709.7	8,709.7	-			
Items Outside of Approved Baseline							7,839.5	7,839.5	-			
Escalation							0.0	0.0	-			
U.S. ATLAS Total		81,104.3	79,406.5	74,677.7	(1,697.8)	4,728.9	163,750.0	163,750.0	-	49.5	48.5	45.6

Notes: 1 LOE

FIGURE 11-1 - MILESTONE SCHEDULE STATUS REPORT

ID	Subsystem ID	Milestone	ETC 01 Baseline	Forecast	Actual
1		Project Start (10/1/95)	Sun 10/1/95	Sun 10/1/95	Sun 10/1/95
2	Tile L2/1	Start Submodule Procurement	Mon 9/1/97	Mon 9/1/97	Mon 9/1/97
3	Tile L2/2	Technology Choice for F/E Electronics	Sat 11/15/97	Sat 11/15/97	Sat 11/15/97
4	LAr L2/1	Cryostat Contract Award	Fri 7/24/98	Wed 8/5/98	Wed 8/5/98
5	LAr L2/2	Barrel FTs Final Design Review	Wed 9/30/98	Fri 10/2/98	Fri 10/2/98
6	TRT L2/1	Final Design Complete	Thu 12/31/98	Mon 12/7/98	Mon 12/7/98
7	LAr L2/4	FCAL Mech Design Complete	Mon 12/14/98	Wed 12/15/99	Wed 12/15/99
8	Tile L2/3	Start Module Construction	Sat 5/1/99	Mon 9/20/99	Mon 9/20/99
9	TDAQ L2/1	Select Final LVL2 Architecture	Fri 12/31/99	Fri 3/31/00	Fri 3/31/00
10	LAr L2/3	Start Elec.'s Production (Preamps)	Fri 6/30/00	Fri 6/30/00	Fri 6/30/00
11	Muon L2/1	Start MDT Chambers Lines 1 & 3	Mon 7/17/00	Fri 9/15/00	Fri 9/15/00
12	Muon L2/6	Kinematic Mount Design Complete	Tue 1/30/01	Tue 1/30/01	Tue 1/30/01
13	Tile L2/4	Start Production of MBs	Sun 4/1/01	Fri 3/30/01	Fri 3/30/01
14	LAr L2/9	Cryostat Arrives at CERN	Tue 5/15/01	Mon 7/2/01	Mon 7/2/01
15	TRT L2/4	Select Final Elec Design	Fri 6/15/01	Wed 8/30/00	Wed 8/30/00
16	Sil L2/1	Start Full Silicon Strip Elec Production	Fri 7/6/01	Sun 7/15/01	Sun 7/15/01
17	Sil L2/6	Pixels '1st IBM Prototype Submitted'	Thu 7/26/01	**Mon 11/12/01**	NA
18	Muon L2/2	Start CSC Chamber Production	Sat 9/1/01	**Mon 10/1/01**	**Mon 10/1/01**
19	Sil L2/3	ROD Design Complete	Mon 10/1/01	**Wed 4/17/02**	NA
20	LAr L2/6	Level 1 Trigger Final Design Complete	Thu 10/4/01	**Sat 3/30/02**	NA
21	Muon L2/3	MDT Electronics ASD PRR	Fri 10/19/01	**Thu 1/31/02**	NA
22	Sil L2/2	Start Full Strip Module Production	Mon 1/7/02	**Fri 3/15/02**	NA
23	TRT L2/5	Start Production of ASICS	Fri 1/18/02	Fri 1/18/02	NA
24	LAr L2/10	Barrel FTs Production Complete	Fri 2/15/02	**Sat 6/1/02**	NA
25	Muon L2/4	Final Design of Global Align Devices	Mon 4/1/02	Mon 4/1/02	NA



ID	Subsystem ID	Milestone	ETC 01 Baseline	Forecast	Actual
26	Muon L2/5	CSC IC Production Complete	Wed 5/15/02	Wed 5/15/02	NA
27	LAr L2/8	MB System Production Complete	Sun 6/30/02	Sun 6/30/02	NA
28	TDAQ L2/3	LVL2 Trigger Prototype Complete	Mon 9/30/02	Mon 9/30/02	NA
29	Tile L2/6	Module Construction Complete	Mon 9/30/02	Mon 9/30/02	NA
30	Tile L2/5	All Elec.'s Components Delivered to ATLAS	Tue 10/1/02	Tue 10/1/02	NA
31	LAr L2/11	FCAL-C Delivered to EC	Thu 10/17/02	Thu 10/17/02	NA
32	Tile L2/7	All Modules Delivered to CERN	Mon 12/2/02	Mon 12/2/02	NA
33	LAr L2/7	ROD Final Design Complete	Thu 12/12/02	Thu 12/12/02	NA
34	TDAQ L2/2	LVL2 Trigger Design Complete	Tue 12/31/02	Tue 12/31/02	NA
35	TDAQ L2/4	Start Production	Wed 1/8/03	Wed 1/8/03	NA
36	TDAQ L2/5	Start Installation & Commissioning	Wed 3/5/03	Wed 3/5/03	NA
37	Muon L2/10	MDT Elec.'s Mezz Production Complete	Thu 3/6/03	Thu 3/6/03	NA
38	Sil L2/7	Pixels 'Start IBM Production'	Thu 3/13/03	Thu 3/13/03	NA
39	TRT L2/2	Module Production Complete (CUM 102)	Mon 3/31/03	Mon 3/31/03	NA
40	Sil L2/5	ROD Production/Testing Complete	Tue 6/24/03	Tue 6/24/03	NA
41	TRT L2/3	Barrel Construction Complete	Tue 9/16/03	Tue 9/16/03	NA
42	Sil L2/4	Compl Shipment of Silicon Strip Modules Prod	Mon 10/13/03	Mon 10/13/03	NA
43	Sil L2/8	Pixels 'Start IBM Outer Bare Module Prod'	Wed 10/22/03	Wed 10/22/03	NA
44	Muon L2/9	CSC ROD Production Complete	Wed 11/5/03	Wed 11/5/03	NA
45	LAr L2/12	FCAL-A Delivered to EC	Mon 12/8/03	Mon 12/8/03	NA
46	Muon L2/8	Kinematic Mount Production Complete	Mon 5/24/04	Mon 5/24/04	NA
47	Muon L2/7	MDT Chambers (U.S.) Prod Compl (Qty. 240)	Fri 8/27/04	Tue 9/14/04	NA
48	Muon L2/12	Global Align System Final Delivery	Thu 9/30/04	Thu 9/30/04	NA
49	Sil L2/9	Pixels 'Disk System at CERN'	Wed 10/13/04	Wed 10/13/04	NA
50	Muon L2/11	CSC Assembly/Test at CERN Complete	Fri 12/17/04	Fri 12/17/04	NA
51	TRT L2/6	Installation Complete	Tue 1/4/05	Tue 1/4/05	NA
52	TDAQ L2/6	Production Complete	Sat 7/30/05	Sat 7/30/05	NA
53	TDAQ L2/7	Installation & Commissioning Complete	Fri 9/30/05	Fri 9/30/05	NA

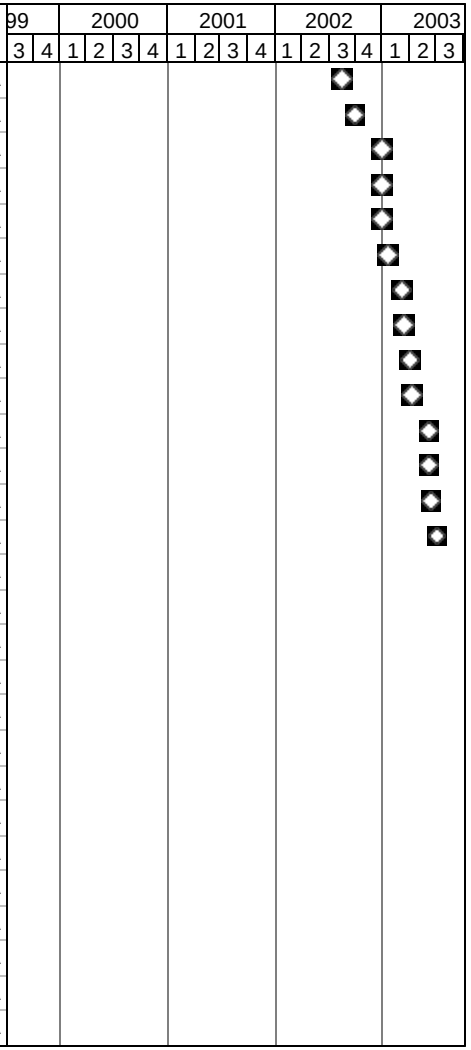
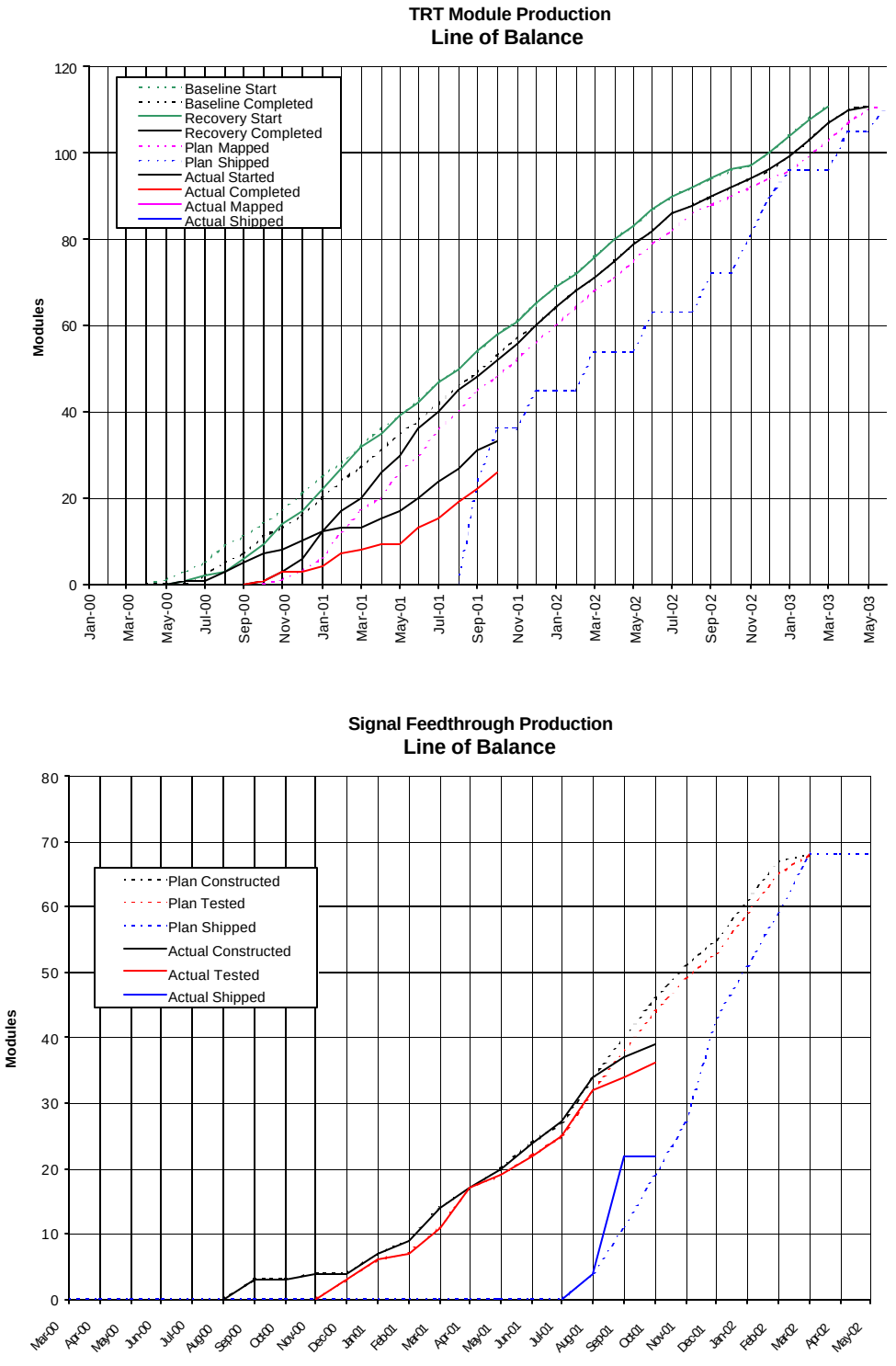


FIGURE 11-2 - LINE OF BALANCE THROUGH OCTOBER 2001



12. MILESTONE LOG

The milestones have been updated with the new ETC 01 baseline dates.

U.S. ATLAS Major Project Milestones (Level 1)

Description	Baseline Schedule	Forecast (F) Date	Actual (A) Date
Project Start	01-Oct-95	01-Oct-95 (F)	01-Oct-95 (A)
Project Completion	30-Sep-05	30-Sep-05 (F)	

U.S. ATLAS Major Project Milestones (Level 2)

Subsystem	**Schedule Designator**	**Description**	**Baseline Schedule**	**Forecast (F) / Actual (A) Date**
Silicon (1.1)	SIL L2/1	Start Full Silicon Strip Electronics Production	06-Jul-01	15-Jul-01 (A)
	SIL L2/2	Start Full Strip Module Production	07-Jan-02	**15-Mar-02 (F)**
	SIL L2/3	ROD Design Complete	01-Oct-01	**17-Apr-02 (F)**
	SIL L2/4	Complete Shipment of Silicon Strip Module Production	13-Oct-03	13-Oct-03 (F)
	SIL L2/5	ROD Production/Testing Complete	24-Jun-03	24-Jun-03 (F)
	SIL L2/6	Pixels 1st IBM Prototype Submitted	26-Jul-01	**12-Nov-01 (F)**
	SIL L2/7	Pixels Start IBM Production	13-Mar-03	13-Mar-03 (F)
	SIL L2/8	Pixels Start IBM Outer Bare Module Prod	22-Oct-03	22-Oct-03 (F)
	SIL L2/9	Pixels Disk System at CERN	13-Oct-04	13-Oct-04 (F)
TRT (1.2) Mechanical	TRT L2/1	Final Design Complete	31-Dec-98	07-Dec-98 (A)
	TRT L2/2	Module Production Complete (CUM 102)	31-Mar-03	31-Mar-03 (F)
	TRT L2/3	Barrel Construction Complete	16-Sep-03	16-Sep-03 (F)
Electrical	TRT L2/4	Select Final Elec Design	15-Jun-01	30-Aug-00 (A)
	TRT L2/5	Start Production of ASICS	18-Jan-02	18-Jan-02 (F)
	TRT L2/6	Installation Complete	04-Jan-05	04-Jan-05 (F)
LAr Cal (1.3)	LAr L2/1	Cryostat Contract Award	24-Jul-98	05-Aug-98 (A)
	LAr L2/2	Barrel Feedthroughs Final Design Review	30-Sep-98	02-Oct-98 (A)
	LAr L2/3	Start Electronics Production (Preamps)	30-Jun-00	30-Jun-00 (A)
	LAr L2/4	FCAL Mechanical Design Complete	14-Dec-98	15-Dec-99 (A)
	LAr L2/6	Level 1 Trigger Final Design Complete	04-Oct-01	**30-Mar-02 (F)**
	LAr L2/7	ROD Final Design Complete	12-Dec-02	12-Dec-02 (F)
	LAr L2/8	Motherboard System Production Complete	30-Jun-02	30-Jun-02 (F)
	LAr L2/9	Cryostat Arrives at CERN	15-May-01	02-Jul-01 (A)
	LAr L2/10	Barrel Feedthroughs Production Complete	15-Feb-02	**1-Jun-02 (F)**
	LAr L2/11	FCAL-C Delivered to EC	17-Oct-02	17-Oct-02 (F)
	LAr L2/12	FCAL-A Delivered to EC	08-Dec-03	08-Dec-03 (F)

Subsystem	Schedule Designator	Description	Baseline Schedule	Forecast (F) / Actual (A) Date

U.S. ATLAS Major Project Milestones (Level 2) (Continued)

Subsystem	Schedule Designator	Description	Baseline Schedule	Forecast (F) / Actual (A) Date
Tile Cal (1.4)	Tile L2/1	Start Submodule Procurement	01-Sep-97	01-Sep-97 (A)
	Tile L2/2	Technology Choice for F/E Electronics	15-Nov-97	15-Nov-97 (A)
	Tile L2/3	Start Module Construction	01-May-99	20-Sep-99 (A)
	Tile L2/4	Start Production of Motherboards	01-Apr-01	30-Mar-01 (A**)**
	Tile L2/5	All Electronic Components Delivered to CERN	01-Oct-02	01-Oct-02 (F)
	Tile L2/6	Module Construction Complete	30-Sept-02	30-Sep-02 (F)
	Tile L2/7	All Modules Delivered to CERN	02-Dec-02	02-Dec-02 (F)
Muon (1.5)	Muon L2/1	Start MDT Chambers Lines 1 and 3	17-Jul-00	15-Sep-00 (A)
	Muon L2/2	Start CSC Chamber Production	01-Sep-01	**01-Oct-01 (A)**
	Muon L2/3	MDT Electronics ASD PRR	19-Oct-01	**31-Jan-02 (F)**
	Muon L2/4	Final Design of Global Alignment Devices Complete	01-Apr-02	01-Apr-02 (F)
	Muon L2/5	CSC IC Production Complete	15-May-02	15-May-02 (F)
	Muon L2/6	Kinematic Mount Design Complete	30-Jan-01	30-Jan-01 (A)
	Muon L2/7	MDT Chambers (U.S.) Production Complete	27-Aug-04	14-Sep-04 (F)
	Muon L2/8	Kinematic Mount Production Complete	24-May-04	24-May-04 (F)
	Muon L2/9	CSC ROD Production Complete	05-Nov-03	05-Nov-03 (F)
	Muon L2/10	MDT Elec.'s Mezzanine Production Complete	06-Mar-03	06-Mar-03 (F)
	Muon L2/11	CSC Assembly/Testing at CERN Complete	17-Dec-04	17-Dec-04 (F)
	Muon L2/12	Global Alignment System Final Delivery	30-Sep-04	30-Sep-04 (F)
Trigger/ DAQ (1.6)	TDAQ L2/1	Select Final LVL2 Architecture	31-Dec-99	31-Mar-00 (A)
	TDAQ L2/2	LVL2 Trigger Design Complete	31-Dec-02	31-Dec-02 (F)
	TDAQ L2/3	LVL2 Trigger Prototype Complete	30-Sep-02	30-Sep-02 (F)
	TDAQ L2/4	Start Production	08-Jan-03	08-Jan-03 (F)
	TDAQ L2/5	Start Installation & Commissioning	05-Mar-03	05-Mar-03 (F)
	TDAQ L2/6	Production Complete	30-Jul-05	30-Jul-05 (F)
	TDAQ L2/7	LVL2 Installation & Commissioning Complete	30-Sep-05	30-Sep-05 (F)

U.S. ATLAS Major Project Milestones (Level 4)

WBS	Schedule Designator	U.S. ATLAS Responsibility Completion Description	ETC01 Baseline Scope Planned Completion Date	Forecast (F)/ Actual (A) Baseline Scope Completion Date	ATLAS Required Date	Baseline Scope Planned Float (Months)
Silicon						
1.1.2	Sil L4/1	Complete Shipping of Silicon Strip Prod Modules	10/03	10/03	4/03	-6
1.1.3	Sil L4/2	RODs 45% Production Complete	9/02	9/02	6/03	9
1.1.1	Sil L4/3	Pixels 'Disk System at CERN'	10/04	10/04	12/04	2
TRT						
1.2.1	TRT L4/1	Barrel Modules Ship to CERN Complete	8/02	8/02	3/03	7
1.2.5	TRT L4/2	ASDBLRs Ship to LUND Complete	10/02	10/02	11/02	1
	TRT L4/3	ASDBLRs Ship to CERN Complete	11/02	11/02	12/02	1
	TRT L4/4	PCB-Endcaps Ship to CERN Complete	4/03	4/03	10/03	6
LAr						
1.3.1	LAr L4/1	Cryostat Final Acceptance Test Complete	8/01	8/01 (A)	11/01	3
1.3.2	LAr L4/2	Signal FT Installation Complete	11/02	11/02	10/02	-1
	LAr L4/3	HV FT End-Cap C Install Complete	2/02	2/02	11/01	-3
	LAr L4/4	HV FT Barrel Install Complete	11/01	11/01	5/02	6
	LAr L4/5	HV FT End-Cap A Install Complete	12/02	12/02	9/02	-3
1.3.3	LAr L4/6	LAr Cryogenics Vendor Install Complete	9/03	9/03	12/03	3
1.3.4.1	LAr L4/7	Last Del of Readout Electrodes	12/02	12/02	10/02	-2
1.3.4.2	LAr L4/8	MBs Ship to Annecy,Saclay (France)	6/02	6/02	9/02	3
1.3.5.1	LAr L4/9	Preamp Deliveries to FEB Complete	5/03	5/03	3/04	10
1.3.5.2	LAr L4/10	Prec Calor Calib Production Complete	N/A	N/A	N/A	N/A

U.S. ATLAS Major Project Milestones (Level 4) (Continued)

WBS	Schedule Designator	U.S. ATLAS Responsibility Completion Description	ETC01 Baseline Scope Planned Completion Date	Forecast (F)/ Actual (A) Baseline Scope Completion Date	ATLAS Required Date	Baseline Scope Planned Float (Months)
Lar (Continued)						
1.3.6.1	LAr L4/12	Pedestal Ship to CERN Complete	12/01	12/01	7/02	7
	LAr L4/13	Barrel Ship to CERN Complete	12/01	12/01	3/03	15
1.3.6.2	LAr L4/14	Cables Shipping Complete	10/02	10/02	3/03	5
	LAr L4/15	Baseplane Last Delivery to CERN Complete	10/02	10/02	3/03	5
1.3.6.3	LAr L4/16	EC Crates Last Delivery to CERN Complete	10/02	10/02	3/03	5
	LAr L4/17	Barrel Crates Last Delivery to CERN Complete	10/02	10/02	3/03	5
1.3.6.4	LAr L4/18	Controls Ship to CERN Complete	9/03	9/03	5/04	8
	LAr L4/19	Power Supplies Last Delivery Complete	9/04	9/04	5/04	-4
1.3.6.5	LAr L4/21	Thermal Contacts (Proto) Last Delivery Complete	9/02	9/02	9/02	0
1.3.7.1	LAr L4/22	FEB Last Delivery Complete	8/04	8/04	1/05	5
1.3.7.4	LAr L4/24	Last Driver Delivery to FEB Complete	4/04	4/04	5/04	1
1.3.8.1	LAr L4/26	Layer Sums Last Delivery to FEB Complete	12/02	12/02	3/04	15
1.3.8.2	LAr L4/27	I/F to Level 1 Ship to CERN Complete	8/04	8/04	12/04	4
1.3.9	LAr L4/28	ROD System Final Prototype Complete	8/02	8/02	8/02	0
1.3.10	LAr L4/29	Deliver Finished FCAL-C to EC	10/02	10/02	10/02	0
	LAr L4/30	Deliver Finished FCAL-A to EC	12/03	12/03	11/03	-1
	LAr L4/31	FCAL Elec.'s Summ Bds Ready for Installation	12/01	12/01	2/02	2
	LAr L4/32	FCAL Elec.'s Cold Cables Testing Complete	11/01	11/01	2/02	3

U.S. ATLAS Major Project Milestones (Level 4) (Continued)

WBS	Schedule Designator	U.S. ATLAS Responsibility Completion Description	ETC01 Baseline Scope Planned Completion Date	Forecast (F)/ Actual (A) Baseline Scope Completion Date	ATLAS Required Date	Baseline Scope Planned Float (Months)
Tile						
1.4.1	Tile L4/1	Submodules Construction Compl (Original Baseline Scope –Qty. 45)	7/01	3/01 (A)	8/01	5
	Tile L4/2	EB Module Ship to CERN Complete (Qty. 40)	12/01	12/01	7/02	7
1.4.2	Tile L4/3	Optics Instrumentation at ANL & MSU Complete	9/02	9/02	11/02	2
1.4.3	Tile L4/4	PMT Ship to ATLAS Complete	1/02	1/02	7/02	6
1.4.3	Tile L4/5	Readout Ship to ATLAS Complete	11/02	11/02	3/03	4
1.4.4	Tile L4/6	Gap Submodules Ship to ANL & BCN Compl (Original Baseline Scope-Qty. 77)	7/01	4/01 (A)	8/01	4
1.4.1	Tile L4/7	Submodule Construction Compl (Qty. 576)	3/02	3/02	7/02	4
1.4.1	Tile L4/8	EB Module Ship to CERN Complete (Qty. 64)	12/02	12/02	1/03	1
1.4.4	Tile L4/9	Gap Submodules Ship to ANL & BCN Compl (Qty. 128)	7/02	7/02	7/02	0

Muon						
1.5.7 (1)	Muon L4/1	MDT Chamber Prod Complete (BMC Qty. 80)	6/04	6/04	2/04	-4
		MDT Chamber Prod Complete (Mich Qty. 80)	8/04	8/04	2/04	-6
		MDT Chamber Prod Complete (Seattle Qty. 80)	8/04	8/04	2/04	-6
1.5.8 (2)	Muon L4/2	MDT Mounts Prod Complete/Delivered to Chambers	10/03	10/03	2/04	4
1.5.9 (3)	Muon L4/3	MDT Elec.'s Mezzanine Bd Production Complete	3/03	3/03	2/03	-1
	Muon L4/4	MDT Elec.'s Hedgehog Production Complete	12/01	12/01	4/01	-8
1.5.4	Muon L4/5	CSC Chambers Production Complete	1/03	1/03	4/04	15
1.5.11 (5)	Muon L4/6	ASMs Production Complete	4/04	4/04	4/04	0
	Muon L4/7	Sparsifiers Ship to CERN	3/04	3/04	10/04	7
	Muon L4/8	RODs Ship to CERN	3/04	3/04	10/04	7
	Muon L4/9	Support Electronics Ship to CERN	3/04	3/04	10/04	7
1.5.12 (6)	Muon L4/10	Align Bars Ship to CERN	3/04	3/04	12/04	9
	Muon L4/11	Proximity Monitors Ship to CERN	12/03	12/03	12/04	12
	Muon L4/12	Multi-Point System Ship to CERN	3/03	3/03	3/05	24
	Muon L4/13	DAQ Ship to CERN	9/04	9/04	12/04	3
Trig/DAQ						

13. NSF COST SCHEDULE STATUS REPORT

Fourteen US ATLAS institutions will receive funding under the NSF Cooperative Agreement (No. PHY 9722537) in 2001. Technical progress reports are given in the respective subsystem paragraphs of Section 4. The NSF Cost Schedule Status Report (CSSR) in this section covers these 14 institutions, in addition to the Education, Institutional Dues and Common Project items which will be funded by the NSF, and also the Items Outside Approved Baseline and Contingency.

Status through the month of October 2001 reflects the ETC 01 baseline schedules for all subsystems. The schedules are resource-loaded to the baseline funding of $163,750K with Contingency, Management Contingency and Items Outside of the Approved Baseline shown on separate lines, excluding all NSF R&D funds. The anticipated NSF contribution to the baseline funding is $60,800K

We note that more than half of the universities in the NSF CSSR are, or have been, funded by both NSF and DOE, while we manage the project without distinguishing the agency source of funding. For this reason, the NSF+DOE Budgeted AY$s column in Table 13-1 includes all Project funds allocated to each institution, while the last two columns to the far right show the contribution of each agency.

The re-baseline date was established as October 1 2000 and the FY 01 Estimate to Complete (ETC-01) was defined as all tasks and resources required too complete the project. These tasks were scheduled and the necessary resources were loaded into the schedules. All prior efforts were equated to the actual cost expended. There was a negative schedule variance along with a positive cost variance in the old baseline and this resulted in a reduction in both the work scheduled and the work performed in the new baseline.
The CSSR shows that $28,340.5K of the work has been completed which represents approximately 49.8% of the work authorized to date. There is an unfavorable schedule variance of $581.0 or 2.0% behind the plan and a favorable cost variance of $322.6K or 1.1% under spent for the work accomplished. There are outstanding commitments of $617.6k at this time that do not show up in the performance.

Schedule Variance

Hampton – SV = ($273.6k)

WBS 1.2.1.1.3 Barrel Module Component Assembly is behind plan $273.6k

Cost Variance

Although the overall cost variance for NSF Institutions is a favorable $767.2k it is comprised of both positive and negative variances as follows:

- Brandeis – CV = ($290.5k)
  - Over spent on tooling ($58.0k)
  - Charging against Global System Production tasks ($144.0k)
- Harvard – CV = ($87.8k)
- Nevis – CV = ($156.5K)
  - Over spent on the FEB ($198.7k)
  - Offset by small positive CV in the ROD System and Beam Tests
- MSU CV = $41.3K

- UCI CV = $44.4k
- UCSC CV = $256.6k
  - The Silicon Strip System is under spent in the area of Design, Development and Prototypes
- University of Rochester CV = $163.3K
  - Under spent by $151.6k on Vendor Manufacturing but shows an outstanding commitment of $178.4k
- University of Texas at Arlington CV = $432.2K
  - Under spent on Intermediate Tile Calorimeter Production
- University of Chicago CV = $103.0K
  - Under spent on Readout and Front End Motherboards by $33.6k and $77.8k respectively
  - Over spent by ($26.5k) Extended Barrel Module
- University of Washington CV = ($244.7k)

Table 13

Cost Schedule Status Report

Reporting Period Ending:9/30/01

Institution	Cumulative To Date (k$)					At Completion (k$)			Complete (%)			Budgeted AY $s	
	Budgeted Cost		Actual Cost	Variance		NSF + DOE	Latest						
	Work Scheduled	Work Performed	Of Work Performed	Schedule	Cost	Budgeted AY $s	Revised Estimate	Variance	Scheduled	Performed	Actual	NSF	DOE
Brandeis	1,905.1	1,897.8	2,188.3	(7.3)	(290.5)	2,848.5	2,848.5	-	66.9	66.6	76.8	2,413.3	435.2
Harvard	3,204.4	3,195.7	3,283.5	(8.7)	(87.8)	6,909.4	6,909.4	-	46.4	46.3	47.5	6,909.4	
Columbia Nevis Lab [2]	3,960.1	3,952.5	4,109.0	(7.6)	(156.5)	9,458.1	9,458.1	-	41.9	41.8	43.4	9,196.8	261.3
Hampton University	1,341.9	1,068.3	1,074.0	(273.6)	(5.7)	1,495.3	1,495.3	-	89.7	71.4	71.8	1,495.3	
Michigan State University	714.7	673.4	632.1	(41.3)	41.3	1,075.5	1,075.5	-	66.5	62.6	58.8	1,040.2	35.3
Oklahoma	177.2	176.7	148.3	(0.5)	28.4	393.7	393.7	-	45.0	44.9	37.7	342.3	51.4
Pittsburg	666.3	624.7	585.9	(41.6)	38.8	2,033.6	2,033.6	-	32.8	30.7	28.8	1,920.1	113.5
SUNY Stony Brook	1,469.8	1,450.1	1,450.3	(19.7)	(0.2)	1,089.1	1,089.1	-	135.0	133.1	133.2	1,083.9	5.2
University of California Irvine	741.3	661.9	617.5	(79.4)	44.4	2,010.4	2,010.4	-	36.9	32.9	30.7	1,715.8	294.6
University of California Santa Cruz	3,628.2	3,623.7	3,367.1	(4.5)	256.6	3,984.5	3,984.5	-	91.1	90.9	84.5	3,286.3	698.2
University of Rochester	5,848.1	5,848.1	5,684.8	-	163.3	9,287.6	9,287.6	-	63.0	63.0	61.2	8,936.7	350.9
University of Texas Arlington	1,550.4	1,532.1	1,099.9	(18.3)	432.2	1,534.7	1,534.7	-	101.0	99.8	71.7	1,431.0	103.7
University of Chicago	2,098.2	2,089.6	1,986.6	(8.6)	103.0	2,126.9	2,126.9	-	98.6	98.2	93.4	2,115.4	11.5
Washington	1,617.8	1,545.9	1,790.6	(71.9)	(244.7)	3,241.0	3,241.0	-	49.9	47.7	55.2	3,241.0	
Education [3]				-	-	286.5	286.5	-	-	-	-	286.5	
Institutional Dues [3]				-	-	2,036.6	2,036.6	-	-	-	-	1,930.4	106.2
Common Projects [3]				-	-	7,142.5	7,142.5	-	-	-	-	652.2	6,490.3
Sub Total	28,921.5	28,340.5	28,017.9	(581.0)	322.6	56,953.9	56,953.9	-	50.8	49.8	49.2	47,996.6	
								-				-	
Items outside baseline						2,388.5	2,388.5	-				2,388.5	
Management Contingency						4,921.7	4,921.7	-				4,921.7	
Contingency						4,219.9	4,219.9	-				4,219.9	
Project Management						1,273.3	1,273.3	-				1,273.3	
							-						
Total (with DOE Funds included)	28,921.5	28,340.5	28,017.9	(581.0)	322.6	69,757.3	69,757.3	-	41.5	40.6	40.2		8,957.3
Total NSF Funds												60,800.0	

Note
1. Not used
2. Nevis Costs do not currently include Project management costs
3. Treated as LOE based on actuals reported

	60,800.0	69,757.30
	-	

14. DETAILED TECHNICAL PROGRESS

1.1 SILICON

Milestones with changed forecast dates:

1.1.1.1.1 Design

Milestone	Baseline	Previous	Forecast	Status
ATLAS PM approval of Support tube procurement	5-Mar-02	5-Mar-02	15-Dec-02	Delayed (See #1)

Note #1 Design scope increased to support beam pipe, many interfaces to be resolved with other systems.

1.1.1.1.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Support tube development complete	10-Dec-01	1-May-02	15-Jun-02	Delayed (See #1)

Note #1 Design scope increased to support beam pipe, many interfaces to be resolved with other systems. Critical interface to SCT likely to change significantly.

1.1.1.2.1 Design

Milestone	Baseline	Previous	Forecast	Status
ATLAS PM approval of production procurement	23-Jul-01	1-Oct-01	10-Dec-01	Delayed (See #1)
Release initial MC for sensors/testing	23-Jul-01	1-Oct-01	1-Dec-01	Delayed (See #2)

Note #1-2 Production is planned to begin in January 2002. Since there is considerable slack in the sensor schedule, this has no impact on the global schedule.

1.1.1.3.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
1st IBM prototype submitted (FE-I1)	26-Jul-01	26-Oct-01	12-Nov-01	Delayed (See #1)
1st IBM prototype delivered	24-Oct-01	2-Jan-02	19-Jan-02	Delayed (See #2)
Complete initial wafer probe FE-I1	7-Nov-01	18-Jan-02	1-Feb-02	Delayed (See #3)
First bump bonded FE-I1 assemblies arrive	9-Jan-02	1-Mar-02	15-Mar-02	Delayed (See #4)

Note #1 This milestone has finally been completed, but the milestone editor considers the date of completion to be too late for this report.

Note #2-3 Note that due to reduced foundry demand, the turnaround for IBM has been observed to be as low as 5 weeks, so the 8-week processing time assumed here should be reasonable. However, wafers must be shipped through CERN under present frame contract, and CERN closes for two weeks around Christmas holiday period, delaying estimated delivery into early 2002.

Note #4 See Note #2 above. We are assuming a 6-week turnaround for the bump-bonding vendor. Significant processing of dummy wafers will be performed first to validate the processing of 8" wafers.

1.1.2.1.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Test Systems Complete	3-Aug-01	31-Oct-01	31-Dec-01	Delayed (See #1)

Note #1 The wafer test systems are operational and qualified for production. Some work is continuing to reduce test time and add some improved tests. The new tests and revised test spec is complete. The qualification of the new tests was postponed until after the first production delivery of 35 wafers was tested so as to not hold up production schedule. The qualification of the new tests was not completed in October but is continuing. Also, work is ongoing to complete the spare parts for test systems. It is expected that all will be completed by year-end.

1.1.2.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
1st Preproduction Hybrids Avail for Mod Assy	4-Jun-01	15-Oct-01	15-Dec-01	Delayed (See #1)
Compl Preproduction Assy	13-Aug-01	21-Nov-01	21-Jan-02	Delayed (See #2)
Compl Testing of Preprod Hybrid	3-Sep-01	21-Nov-01	21-Feb-02	Delayed (See #3)

Note #1 This will follow the hybrid design review and is set by Japanese procurement schedule. The FDR is complete but some minor mods have been circulated. We have not received word that the hybrids are available from the Japanese.
Note #2-3 Set by date of item1 above.

1.1.2.3.1 Design of Assembly & Test Tooling

Milestone	Baseline	Previous	Forecast	Status
Module PRR	3-Sep-01	1-Mar-02	8-Mar-02	Delayed (See #1)
Compl Design of Preprod Mod Assy/Test	3-Sep-01	3-Nov-01	3-Feb-02	Delayed (See #2)

Note #1 Given the delay discussed in #1 above this is the current expected date for the US module assembly PRR.
Note #2 Now that the fixation point is settled fixtures have to be modified and tested.

1.1.2.3.3 Production

Milestone	Baseline	Previous	Forecast	Status
Complete Preproduction Module Assembly	30-Jul-01	30-Jan-02	1-Mar-02	Delayed (See #1)
Complete Preproduction Module Testing	3-Sep-01	15-Feb-02	15-Mar-02	Delayed (See #2)
Start Full Strip Module Production	7-Jan-02	1-Mar-02	15-Mar-02	Delayed (See #3)

Note #1-2 Require pre-production hybrids which are still unavailable from Japan. Requires validation of new fixtures now that fixation point is settled.
Note #3 Defined as date of module assembly PRR.

1.1.3.4.3 SCT/Pixel Test Stand Software

Milestone	Baseline	Previous	Forecast	Status
Production Diagnostic Test Stand Completed	29-Sep-00	29-Oct-01	29-Apr-02	Delayed (See #1)

Note #1 The test stand software is completely functional for the production testing. This software will be updated for more efficiency in the next few months. The minor improvements to the software will continue till the mid part of FY 02.

1.1.3.6.3 User Evaluation of ROD in Europe

Milestone	Baseline	Previous	Forecast	Status
SCT ATLAS Final Design Review	11-Jun-01	15-Nov-01	15-May-02	Delayed (See #1)
Pixel ATLAS Final Design Review	1-Jan-02	1-Jan-02	1-May-02	Delayed (See #2)

Note #1 The new schedule forecast a date of 4/3/02 for this review. At that time the BOC and ROD should be ready for the review.
Note #2 The current new schedule predicated on user evaluation assumes the review will be late in FT 02.

1.1.3.7.3 Evaluation of Production Model

Milestone	Baseline	Previous	Forecast	Status
Pixel ROD Design complete	14-Jun-01	15-Nov-01	15-Feb-02	Delayed (See #1)

Note #1 The VHDL is still under development. It is projected to be completed and evaluated by Feb 02.

1.1.3.8.1 ROD 5% Production

Milestone	Baseline	Previous	Forecast	Status
Begin First End Cap SCT Module Ass/Test	25-Nov-01	25-Nov-02	25-Apr-02	Delayed (See #1)
Begin First Barrel SCT Module Ass/Test	27-Dec-01	27-Sep-02	27-Apr-02	Delayed (See #2)

Note #1-2 These dates are not known well because of assembly site slippage.

1.1.1 Pixels **Murdock Gilchriese (Lawrence Berkeley Lab.)**

1.1.1.1 Mechanics

Production of parts for disk sector assembly continues. The order for the preproduction disk support ring was placed. Compliance tests of the prototype endcone were completed at LBL and agree with earlier measurements at HYTEC. We remain on schedule for a PRR of the global support frame in February 2002. The detailed design for prototypes (1 foot long) of the support tube and heaters to be bonded to the tube began.

ATLAS is now moving rapidly to adopt the proposal to support the beam pipe from the pixel support tube. And the U.S. design team has been requested to provide this design on an urgent basis taking into account

the FDR of the beam pipe to occur in February 2002. This activity is an increase in scope beyond the current pixel baseline and clearly the beam pipe must be supported in any case. Design and fabrication funds for this activity are not currently available but urgently needed.

1.1.1.2 Sensors

CIS is fully qualified for production. Tesla is now mostly qualified for production, but additional test data after irradiation are desirable. The collaboration wishes to proceed next month with a 25% production order to CIS and Tesla. The remainder of the order would be placed at the end of FY02 or early FY03. CIS will relocate their production facilities starting in the spring of '02 and will not be able to produce wafers again until later summer. A BCP to release management contingency for sensor production and testing will be generated in November.

1.1.1.3 Electronics

The first IBM submission of the FE, MCC and optical chips was delayed until November. The submission to CERN was made on November 12. CERN will forward to IBM. Work on the test system for the front-end chips is proceeding but the schedule is tight. A fallback solution exists to begin wafer probing when IBM wafers arrive in January.

1.1.1.4 Hybrids

The first batch of flex 3.x failed (this happened for the 2.x version for the current vendor). A new batch was started and should be ready in November.

Another prototype of the optical hybrid board has been designed and submitted. This board will be compatible with both DMILL (no longer a viable option but die exist and IBM optical chips). Preliminary results from irradiations of IBM prototype optical chips indicate these are sufficiently rad-hard.

1.1.1.5 Modules

Thermal cycling of poor-quality In-bumped dummy modules mounted on sectors indicates that the In - bump technology appears robust to thermal cycling. We await the fabrication of more dummy modules with dummy wafers currently at IZM and AMS. The next wafer thinning trials will be made with 8", bumped dummy wafers when they arrive.

1.1.1.1 Mechanics

1.1.1.1.1 Design

Milestone	Baseline	Previous	Forecast	Status
Cables/services CDR	20-Jun-01	--	10-Dec-01	Delayed (See #1)
Support tube CDR	20-Jun-01	--	17-Oct-01	Completed
Global Support FDR	16-Oct-01	--	17-Oct-01	Completed
Release bid for Support tube	4-Dec-01	--	5-Oct-02	Delayed (See #2)
Support tube FDR	10-Dec-01	--	15-Jun-02	Delayed (See #3)
Release bids for support	18-Dec-01	--	5-Oct-02	Delayed (See #4)
Bid evaluation complete for support	12-Feb-02	--	15-Dec-02	Delayed (See #5)
Support tube bid eval complete	12-Feb-02	--	15-Dec-02	Delayed (See #6)
Assembly/Installation CDR	26-Feb-02	--	15-Jun-02	Delayed (See #7)
B-layer CDR	26-Feb-02	--	26-Feb-02	On Schedule
Cables/services FDR	26-Feb-02	--	15-Jun-02	Delayed (See #8)
Global Support PRR	26-Feb-02	--	26-Feb-02	On Schedule
Support tube PRR	26-Feb-02	--	1-Oct-02	Delayed (See #9)
ATLAS PM approval of global support procurement	5-Mar-02	--	5-Mar-02	On Schedule
ATLAS PM approval of Support tube procurement	5-Mar-02	5-Mar-02	15-Dec-02	Delayed (See #10)

Note #1, 8 Gap decision requires some redesign. Uncertainties about voltage regulators.

Note #2-7, 9-10 Design scope increased to support beam pipe, many interfaces to be resolved with other systems.

Neal Hartman (Lawrence Berkeley Lab.)

PIXEL SUPPORT TUBE

Analysis has progressed on the pixel support tube (PST) design, including examination of the stiffness implications on the SCT. In response to SCT concerns that the PST is too stiff in bending, fiberglass forward shells have been modeled in ANSYS, and an approximate factor of 4 reduction in loads exerted on the SCT was calculated. Discussions with SCT engineers indicate that a reduction of this magnitude is acceptable. This reduced stiffness, however, results in increased occurrence of shell vibrational modes, so two additional hoop (circumferential) stiffeners were added to each forward tube. Even with this additional stiffening, the natural frequency of the PST with service masses is only slightly more than 40 Hz. While this is less than ideal, it is considered necessary in order to alleviate fears that the PST will cause undue deflections in the SCT during operation. Soon, the SCT FEA model (currently analyzed with IDEAS at

EPLF in Lausanne) will be incorporated into the PST model at LBL, so that actual constraint conditions at the four-barrel support points can be determined. These reaction loads will in turn be used to re-design the PST mounts, at which point iterative analysis will be used to fine-tune the mount designs and reactions imposed on the SCT interlinks. Meanwhile, prototyping plans are moving forward under the assumption that the forward PST shells and rails will be made from fiberglass.

Sally Seidel (University Of New Mexico)

The original concept of including electrical and optical connectors and fittings for the cooling pipes on Patch Panel 1 was designed and proved to not fit. The design concept was changed to a "tophat" design where the barrel electrical and optical connectors for each of the octants were on a side panel and the b-layer electrical, optical, and cooling connectors along with the barrel cooling connectors were located on the end panel. This design also did not fit in the sense that even though all the connectors could be put onto PP1 everything was too densely packed and impractical from an assembly point of view. The design concept, which is currently in progress, replaces the electrical panel connectors for both the barrel and b-layer signals with slots through which the electrical signals routed on a flex cable will feed through. The optical fibers will also feed through the slots and the only connectors are the cooling pipe fittings.

1.1.1.1.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Complete global support development/prototypes	16-Oct-01	--	16-Oct-01	Completed
Support tube development complete	10-Dec-01	1-May-02	15-Jun-02	Delayed (See #1)

Note #1 Design scope increased to support beam pipe, many interfaces to be resolved with other systems. Critical interface to SCT likely to change significantly.

Neal Hartman (Lawrence Berkeley Lab.)

PIXEL SUPPORT TUBE

Calculations are being done to determine which carbon fiber materials should be ordered for initial friction testing, test tube layups, and materials testing (as well as heater prototypes). With the decision to fabricate fiberglass forward tubes comes the implication that two mandrels will be needed (and by extension, two test mandrels) since the barrel and forward shells will have different CTE's. In addition, since fiberglass laminates have a CTE very near to that of steel, it will be necessary to fabricate the forward shell mandrel from aluminum, in order to assure release after autoclave cure. Thus two sample mandrels (each 16" long) will be necessary, one of steel and one of aluminum, with different diameters in order to allow for the different CTE's. These sample mandrels, in addition to the material needed to layup sample PST shells, will be ordered in November.

COOLING SERVICES

Both Al/Al and Al/PEEK luer lock fittings have been tested through the entire new testing regimen (which includes pressure and thermal cycling). All 4 Al/Al luers tested well, passing all test stages. The Al/PEEK luers fared worse, however, with only 3/6 satisfactorily completing the test sequence. These are being examined to determine whether they leak at the joint, or at the underlying adhesive bond (if it's possible to

determine this). In addition, initial mate/demate testing has been conducted, with good results. There is some concern, however, that the vacuum grease which is applied to the fitting surface will be either degraded by radiation or eliminated by C_3F_8, resulting in binding between the fitting halves. In order to test this, Al/Al lures are being irradiated in C_3F_8 to 25 Mrad, and will then be demated and remated in order to examine their behavior.

Indium fittings undergoing testing in Europe have fared very well in the testing regimen. A calculation of total material in the PST volume has shown that the Luer lock fittings as currently designed are approximately 8 times more massive than the indium fittings. For this reason, it may become necessary to adopt indium fittings throughout the pixel system. In order to retain the luers as a viable first or second choice fitting type, radically downsized luer lock fittings are being considered. Though the indium fittings appear attractive, they have not been tested in aluminum yet, so this must be completed before any decisions as to preferred fitting type can be made. European collaborators plan on conducting testing on aluminum versions of the indium fitting before the December pixel week.

Recent laser welding problems have been traced to a different type of aluminum in recent laser welding attempts. It turns out that the original tubing material was 1060 aluminum, not 3003, as advertised by the supplier. When 3003 extrusions were specially ordered, they obviously behaved differently during welding than the 1060 tubing had. Because this difference was unknown, it derailed all laser welding attempts until a compositional analysis was performed, and the surprising results were obtained. Eventually, our primary laser welder was able to weld even the 3003 aluminum to the test fittings, by slightly modifying the weld geometry. Now that this problem has been solved, we will move ahead with a test fabrication of a bent sector tube, made from the original (and well tested) 1060 aluminum tubing.

Global Support Endcone **Murdock Gilchriese (Lawrence Berkeley Lab.)**

The prototype endcone of the global support was shipped to LBL and mounted on the prototype frame. The fit was excellent. Compliance measurements of the long support tabs for the barrel layers were done to compare with similar measurements done only on the endcone by Hytec. The results are very similar, indicating no additional compliance from mounting on the frame. The prototype program for the endcone is complete.

1.1.1.1.3 Production **Murdock Gilchriese (Lawrence Berkeley Lab.)**

Disk Sectors

The manufacture of the final tooling for disk sector production is continuing steadily. The CNC program for cutting carbon-carbon faceplates is being tweaked to bring all cut dimensions within 1mil of nominal. Ten additional faceplates will be cut and inspected by early November. If these look good, all faceplates will be cut by December. The automated inspection process and data transfer to Excel is working. Work is just starting to learn how to upload data into the production database.

Disk Support Rings

The contract with Hytec for fabrication of C-channels and a preproduction ring was placed at the end of the month. The preproduction ring is scheduled to be completed by April 2002, at which time the production order would be placed.

1.1.1.2 Sensors

1.1.1.2.1 Design

Milestone	Baseline	Previous	Forecast	Status
Compl. Spec for production order release	12-Mar-01	--	1-Nov-01	Delayed (See #1)
ATLAS PM approval of production procurement	23-Jul-01	1-Oct-01	10-Dec-01	Delayed (See #2)
Release initial MC for sensors/testing	23-Jul-01	1-Oct-01	1-Dec-01	Delayed (See #3)

Note #1-3 Production is planned to begin in January 2002. Since there is considerable slack in the sensor schedule, this has no impact on the global schedule.

1.1.1.2.2 Development/Prototypes **Sally Seidel (University Of New Mexico)**

Measurements of the first batch of pre-production wafers were completed. The data were entered into the production database, which is still being debugged. A second batch of production wafers examining a few special conditions was received, and measurements of these began. Manufacturer data on the devices are not always transmitted to the ATLAS institute doing the measurements--this will be corrected. Thus far CiS and Tesla wafers are in good agreement with specifications. A decision was taken to proceed with the CiS order (recognizing that it will involve a 3 month pause April - June for movement of the production facility). Tesla will produce 25% of its production order, at which time final studies of radiation hardness will be possible with test beam data.

1.1.1.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
First Outer production wafers delivered	18-Jan-02	--	18-Jan-02	On Schedule (See #1)

Note #1 CIS only.

1.1.1.3 Electronics

1.1.1.3.1 Design

Milestone	Baseline	Previous	Forecast	Status
FE-I1 spec complete	16-May-01	--	1-Dec-01	Delayed (See #1)

Note #1 Specification has been started, and was supposed to be ready for June review. Testing of Analog Test chip and completion of FE-I has taken priority. Document will be completed after submission

Kevin Einsweiler (Lawrence Berkeley Lab.)

We continue to place all of our design resources on the deep-submicron design effort. The focus this month has been on completing the verification of all designs for the engineering run. We have completed the verification of the FE-I chips. This involved the finalization of the analog designs for this submission, with two different feedback capacitors for the two different designs. The nominal design has Cf=10fF, and a gain of roughly 1.8 times that of the test chip design. The high-gain version has Cf=5fF, and a gain of roughly 3 times the test chip design. These higher gains should result in untuned threshold dispersions of roughly 1000e and 600e respectively. The digital design has been extensively verified using Verilog for functional verification and TimeMill and PowerMill for timing verification. Simulations were performed of a complete column pair and EOC buffer block including all layout parasitics. Simulations have also been performed on a little chip in which only 16 pixels per column and 2 EOC buffers per column pair were left in, in addition to all of the chip level circuitry. This has been simulated also including all layout parasitics (300K FETs and 330K capacitors), testing all of the control and readout integration of the full chip.

We have also completed design rule checking for all of the other designs included in this reticle (there are a total of 9 designs in the reticle). These include three opto-chips from OSU, the new MCC from Genova, a new Analog Test Chip from Bonn, and some other minor test chips. After all of this checking, we have filed the appropriate requests for DRC waivers with CERN and have sent our GDS file to CERN. They will quickly inspect and check everything again, and forward it to IBM. If there are no unpleasant surprised, then we expect that fabrication of our engineering run should begin during the week of Nov. 19. We then expect that we should receive the initial 6 wafers from the engineering run in about the middle of Jan 2002, with the second set of 6 wafers to follow within a few weeks. The actual submission date (Nov 12) is about 3.5 months after the nominal submission date in the baselined US ATLAS pixel schedule (July 26). We expect that this slippage will largely propagate through the present electronics schedule, although every effort will be made to move the submission date for the FE-I2 chip in 2002 back towards the present baseline schedule. The remainder of the schedule will be placed on a much clearer basis once we have preliminary test results from the new engineering run.

As the pinout of the FE-I is now frozen, we are beginning to work on the necessary probe cards and support cards required for testing wafers, single die, and modules. All of these cards need to be updated, because of major changes to the pinout required to meet the production module mechanical envelopes. These cards will all be modified and re-fabricated over the next few months, in order to have everything ready in time for the returning wafers. The cards are all quite simple, requiring about 2-3 days of layout work each. We also have to update the schematic and layout of our support card for the Analog Test Chip in this run (similar, but not identical, to the prototype chips we fabricated in Feb/Mar this year with IBM and TSMC). This may require about one week of work, Finally, one of the small chips included on our IBM engineering run is a small LVDS Buffer chip, similar to one we built with DMILL in the past. This chip allows us to implement all of the active circuitry required for our support cards in a small rad-hard die, making irradiation of pixel chips and modules fairly straightforward. We have designed our new IBM LVDS buffer chip to fit a standard SOIC28 package. This part will be used to provide rad-hard LVDS buffering and LVDS to CMOS conversion at our nominal operating voltage of 2.0V on all of our standard support cards. A probe card will be designed for this chip, and a rapid test procedure will be used to make sure we get packaged parts quickly for use on support cards.

In order to exercise the new generation of chips from IBM to the fullest extent possible, and in particular to develop the capability to label chips as “known good die”, and be sure that this classification will remain true after exposure to the full radiation doses of ATLAS, we are completing our improved test system.

We have continued testing of the first TPLL boards received. This work is now progressing well. The operation of the TPLL with single chips has been fully debugged, and work is beginning on testing the VHDL for communicating with and decoding data from modules with MCC chips. We have accumulated a list of changes which is large enough that it calls for a revision of the present board layout before making the 20 boards that we intend to deliver to the pixel collaboration. However, there is a pressing need to have several test setups based on the new TPLL in service when the FE-I engineering run returns in Jan 02. For this reason, we have completed loading and will soon start debugging of the three PC boards we have now, in order to get them into service. Then in Dec, we will revise the schematics and send out the new board for fabrication. The major needs for testing in the collaboration will occur starting after March 02, when bump-bonded modules based on the new FE-I start to appear in pixel institutions. It should be possible for us to deliver a significant number of the revised production TPLL boards by that time.

The PICT board layout is now progressing well. All chips have been placed since about 10 days, and almost all passive components are now placed. Hand routing of critical signals will start shortly. We expect to submit the design for fabrication just before Thanksgiving. The board will be 12 layers, but does not use any particularly aggressive design rules, so fabrication should be straightforward. The layout was delayed by about 2 weeks due to continuing ROD work by the layout engineer. The VHDL programming for the board has started. The new TPLL-PICT slow-control protocol has been developed, along with almost all of the special commands to control the many chips on the PICT from the TPLL. The host PC programming is also fairly well advanced, based on the evolving command specification. We would presently expect to have a first board working in our lab shortly before Christmas.

With the present FE-I schedule, we are still cautiously optimistic that there will be PICTs with all VHDL and host software support in place in LBL and Bonn in time for initial FE-I wafer testing in roughly the second half of January. However, it is possible to perform first testing of FE-I with the new TPLL and an old PCC card replacing the PICT. This would only allow us to check the core functions of the chip under 40 MHz operation, and not to perform all of the additional characterization provided by the PICT, however this could be acceptable for initial wafer probing. We will also make sure that this backup solution is in place in case the PICT schedule slips further.

K.K. Gan (Ohio State)

VDC-I2 and DORIC-I2 have been submitted to IBM for fabrication. A single-ended pre-amp has also been submitted as a test structure. We expect the delivery of the die in January 2002. Both dice have been simulated from the layout with extracted parasitic capacitance together with the wire bonds. The simulations predict both dice will work with all corner transistor parameters. The DORIC is predicted to work with low input signal (12 μA) even with rather high inductance (5 nH) from the wire bonds. We have now gone back to simulate DORIC-I1 from the extracted layout with parasitic capacitance plus wire bonds with the following parameters, 2 nH of inductance, 0.5 pF of capacitance, and 0.1 Ohm of resistance. The simulation predicts spikes in the pre-amp outputs as observed on the bench but large input signal (~160 μA) are needed to decode the data properly, significantly above what is observed in the lab. The spikes mainly originate from the bypass capacitor at the PIN bias voltage. The bypass is to the analog ground, which is not a quiet ground because this ground is also used by the CMOS and LVDS drivers. Removing the bypass capacitor allows the DORIC to be run with lower input signal (~ 40 μA). These simulations predict that DORIC-I2 will perform much better than DORIC-I1.

We have received five packaged VDC-I1's and DORIC-I1's that were irradiated in the cold box with 24 GeV protons at CERN. For the DORIC, we observe no degradation in the clock duty cycle and PIN

current thresholds for no bit errors. For the VDC, we observe a lost of ~ % in the bright (on) current for a given control current (ISET) and the total current consumption has decreased by ~10% (2-3 mA).

1.1.1.3.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
1st IBM prototype submitted (FE-I1)	26-Jul-01	26-Oct-01	12-Nov-01	Delayed (See #1)
1st IBM prototype delivered	24-Oct-01	2-Jan-02	19-Jan-02	Delayed (See #2)
Complete initial wafer probe FE-I1	7-Nov-01	18-Jan-02	1-Feb-02	Delayed (See #3)
First bump bonded FE-I1 assemblies arrive	9-Jan-02	1-Mar-02	15-Mar-02	Delayed (See #4)

Note #1 This milestone has finally been completed, but the milestone editor considers the date of completion to be too late for this report.

Note #2-3 See Nte #2 above. Note that due to reduced foundry demand, the turnaround for IBM has been observed to be as low as 5 weeks, so the 8-week processing time assumed here should be reasonable. However, wafers must be shipped through CERN under present frame contract, and CERN closes for two weeks around Christmass holiday period, delaying estimated delivery into early 2002.

Note #4 See Note#2 above. We are assuming a 6-week turnaround for the bump-bonding vendor. Significant processing of dummy wafers will be performed first to validate the processing of 8" wafers

1.1.1.4 Flex Hybrids/Optical Hybrids

1.1.1.4.1 Design

Milestone	Baseline	Previous	Forecast	Status
Optical FDR	31-Jan-02	--	15-Feb-02	Delayed (See #1)

Note #1 We have changed the chip foundry from DMILL to IBM in order to satisfy the rad-hard requirement. The tentative new date is June 02 so that we have more results on the IBM chips.

Rusty Boyd (University of Oklahoma)

Flex Hybrid Design (UOK)

We are exploring the use of two more layers in the flex hybrid. This is motivated by results from simulations that indicate that there could be serious problems properly decoupling the digital (VDD) voltage for DSM electronics. The additional layers would not be electrically connected in any way to the original layers. This is accomplished by "cut outs" through what we have come to think off as the flex hybrid. Holes would be opened in the upper flex hybrid over areas such as wire bond pads and solder pads where connections are required to the new flex with VDD and VDD return solid Cu planes. This strategy will minimize additional cost, since one would only need to glue the two flex circuits together. In addition, we believe there is enough in common with the v4 flex hybrid and the addition of a new "power plane" flex that no major changes will be required in the v4 design in order to be compatible with both strategies.

This is important for development for several reasons. First, should the basic v4 flex hybrid not work (see 1.1.1.4.2), we need a fallback design quickly so that construction of modules is not delayed. Even if the FE-I modules work with the basic flex hybrid, we need to evaluate the effect of ground planes vs. bussed power on the performance of modules, as the additional power planes do add to the material in the detector. Basic principles also indicate that decoupling for the analog power only needs to be filtered at the input to the flex hybrid to reduce noise. We need to verify that the flex hybrid modules will operate properly without the local decoupling capacitors at each analog FE input.

The FE design team added many internal decoupling capacitors to the FE-I design to mitigate the input slew rate, but this was not done for the MCC-I. So even if the FE's work properly, the lack of sufficient local decoupling at the MCC (we haven't found a way to do this and respect the envelope) could lead to problems.

A good deal of time was also spent this month documenting the v3 flex hybrid design. The documentation has been greatly expanded in anticipation of the PRR in June 2002. Much of this is generic to v3 and v4, so it is efficient to do this now so that we start getting feedback from the rest of the collaboration.

We also expanded the assembly drawings and documentation. The addition of the frame PCB for handling the flex now makes fully automated assembly of the flex hybrid practical. This requires extra drawings and specifications.

1.1.1.4.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Initial Flex 3.x tests complete	13-Dec-01	--	13-Dec-01	On Schedule

K. K. Gan (Ohio State)

We have received the opto-board that was mounted on the shuttle and irradiated with 24 GeV protons at CERN. There are six optical links in the system but we only managed to get five of them working before the irradiation due to the late delivery of the Taiwan opto-packs. One link was broken in the packing by CERN for the shipment back to OSU. Of the remaining four working links, we observed no increase in the PIN current thresholds for no bit errors.

We have populated a new opto-board with VDC-I1/DORIC-I1's. We monitored the PIN current thresholds of each link for no bit errors as more dice are added and see no increase in the thresholds. This is encouraging news but all the thresholds (50-130 uA) are above the specification (40 uA). This experiment needs to be repeated when we receive the VDC-I2/DORIC-I2. These chips are expected to have lower thresholds so future tests will be more sensitive to threshold degradation.

A new opto-board that is comparable with both VDC-D3/DORIC-D3 and VDC-I1/DORIC-I1 has been designed and submitted for fabrication. We expect delivery of these boards in early November.

Frank Wapler (SUNY Albany)

Flex/Hybrids (Albany)

In our regular videoconferences with Rusty Boyd and Pat Skubic (Oklahoma U.) we discussed the schedules for upcoming tests of populated AFH version 3.

In preparation, we reviewed and practiced our procedures for tests of conductance and electrical breakdowns, and we considered design specifications and ordering of a new probecard and of related hardware.

Frank Wappler (currently postdoc at Albany, planning to leave to BaBar early next year) and Rahmi Bula (grad student at Albany, who will then be in charge of the test setup) have scheduled a visit at Oklahoma U., Norman, to see and practice on a functioning module test setup, to review the tests which will be conducted at Albany in detail, and to return corresponding hardware.

Rusty Boyd (University of Oklahoma)

Flex Hybrid Development (UOK)

As mentioned above, new models and simulations of DSM electronics and the flex hybrid indicate that there could be serious problems. Using a model of the FE as a current sink with a slew rate of 0.25 A/ns to 1 A/ns results in ringing in the anticipated VDD voltage of 2 Vdc of a full 2 Vp-p. Although there is no certainty that these slew rates are in the proper range for FE-I and MCC-I, discussions with the electronics coordinator reveal that they cannot be dismissed, either.

We have modeled a "power plane" flex as described in 1.1.1.4.1. Even at 1 A/ns, local decoupling of VDD is not necessary, with the ripple being below 1% of VDD. This is easy to understand, as the inductance of a trace is proportional to the length times the log (of the thickness divided by the cross sectional area). Using trace widths in the 100 - 500 micron range results in inductances of 10's of nH. The power planes lower the inductance to the femtohenry range. Resistance (another important parameter in the decoupling operation) is also reduced by several orders of magnitude.

The first batch of flex hybrids fabricated at Compunetics failed. They had anticipated this and begun another batch in mid-October. The failure was caused by the Au/Ni plating process. Fine tendrils of Au short most of the wire bond pads, much as in the first batch of v2.1. In addition, the Cu was reduced from 20 microns thickness to 13 microns. It has been established that this, too, is happening during the Au/Ni plating process, which is done by an outside firm. We will be working with Compunetics to finally resolve this issue before the fabrication of v4 begins. The second batch of v3 flex had been sent to Compunetics from plating by the end of October and it was verified that the Au shorts did not occur this time. At the end of October, Compunetics was awaiting repair of the flying probe tester that is used to electrically test the flex circuits. It is expected that the v3 flex circuits will ship in early November.

We have received word that the MRI grant we applied for in cooperation with the University of New Mexico and Langston University has been awarded. However, as of the end of October, we are still awaiting receipt of the funds. This money will be used to purchase important equipment for assembly and test of the flex hybrids. We are also trying to secure funding to expand our clean room to house the automated wire bonder and optical comparator we plan to purchase with these funds. Our existing 12' x 12' clean room is already seriously overcrowded.

We have also made progress on the flex hybrid test system. We received and installed a 45 deg. bonding arm for our manual wire bonder, which greatly enhances our ability to successfully bond the AMS MCC. We successfully wire bonded an AMS MCC to an assembled v2.2 flex hybrid and are using it in the

development of the PixelDAQ based functionality test and VXI based continuity test systems. We have also received quotes on and plan to purchase soon, a probe card for use with v3 and beyond flex hybrids.

These probe cards, in conjunction with an FE-I mounted on a circuit board which mates to the probe card, will allow us to do a complete functionality test of assembled (including MCC) flex hybrid. We have also begun to document and refine the test and assembly procedures for flex hybrids from fabrication to mounting on a module.

1.1.1.4.3 Production

Milestone	Baseline	Previous	Forecast	Status
Start initial production buy of components	13-Dec-01	--	13-Dec-01	On Schedule

1.1.1.5 Modules

1.1.1.5.2 Development/Prototypes — Maurice Garcia-Sciveres (Lawrence Berkeley Lab.)

LBL Module Assembly Status Report for November 12, 2001

Dummy Modules

A total of 4 AMS and 1 IZM dummy modules with flex and mounted on a sector with CGL have been thermal

Cycled between July and October 2001. The summary of the results is:

IZM Module: After 19 thermal cycles to -35C and overnight storage many open chains developed. When it was removed from the sector a chip fell off. X-ray inspection showed many small and poorly formed bumps indicating that this module was probably low quality to begin with.

AMS Modules: 3 of the modules survived or order 30 cycles to -35C with no new open chains. One module developed a single new open chain (after 1 cycle) and no more after 30 more cycles. This module as well as two others had been damaged during shipping. Damage included chips falling off. This particular module had 3 chips fall off during shipping prior to thermal cycling.

Hot Modules

The two IZM working hot modules mounted on the same sector have been operated simultaneously. No obvious effect is seen on one module from the operation of the other. However, one of these modules has high noise and the other has a large sensor leakage current.

Dummy Wafers

6 wafers are being bumped and made into modules at IZM and 5 at AMS. At least two bumped wafers from each vendor will be returned to LBNL for thinning (and probably dicing).

Wafer Thinning

No new wafers have been thinned. Waiting for the bumped 8" wafers to arrive.

PP0

The layout of a version 2 prototype of PP0 is on hold pending evolution of the optoboard power requirements. Because of the low supply voltage of DSM opto chips it will probably be necessary to have separate voltages for both PIN and VECSEL.

PP1

Preliminary layouts of the PP1 region have shown that there is a space problem for fitting all electrical, optical and cooling connections. The latest concept for electrical connectors is to use flex pigtails that can be bent outwards onto the flange with surface mount connectors. Finding bulkhead type optical connectors is presently the biggest problem. There is no PP1 solution yet.

Equipment

A used K&S 1470 wirebonder has been purchased. Delivery is expected December 10.

1.1.2 Silicon Strip System — Abe Seiden (University Of Calif. At Santa Cruz)

ATMEL delivered their second batch of wafers on time. These are being tested. In addition the test program is still being optimized to reduce testing time, although we are able to test the planned two wafers a day. The source of excess current on some of the chips is understood as coming from one type of structure where two transistors are very close together. The primary direction with regard to this is to make sure the power supply system can handle the largest currents we have seen and to work on finding potential problem wafers through radiation testing. We need to continue to work on this problem.

Work on modules and hybrids is continuing. Several modules were constructed at LBNL to exercise the system - although the tooling isn't final. Various fixtures are under construction. Also, the removal of bad chips from hybrids is being practiced and appropriate fixtures developed through the experience gained. We are working on developing a short-term plan to begin production of loaded and tested hybrids starting early in January. The goal would be to get a head start on this and also to avoid overlapping the learning curves for both hybrid and module construction.

1.1.2.1 IC Electronics

1.1.2.1.1 Design

Milestone	Baseline	Previous	Forecast	Status
Release management contingency	1-Feb-02	--	1-Feb-02	On Schedule

Alexander A. Grillo (University Of Calif. At Santa Cruz)

LBNL & UCSC

The final planned version of the "on-line" test program, which incorporates some new tests on the I/O functions of the ABCD and also makes other changes to reduce test time, was finished but has not yet been qualified for production. The test time of the new version is approximately 4.5 hours, which will make

a big improvement to the production throughput. Preliminary re-tests of 2 wafers using the new tests, however, gave results different from the present production version. The cause of the differences is still be investigating so qualification is postponed until that is resolved.

The Final Design Review of the SCT harness and optical components was successfully completed on 19-Oct., however, the FDR of the power supplies and transmission system was postponed. The designs were not sufficiently complete to warrant an FDR. Instead an internal review of the whole system was held with just the engineers and physicists responsible for its design. Ned Spencer and Alex Grillo attended both meetings. Some progress has been made, but continued oversight will be necessary to keep this work on course.

1.1.2.1.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Test Systems Complete	3-Aug-01	31-Oct-01	31-Dec-01	Delayed (See #1)

Note #1 The wafer test systems are operational and qualified for production. Some work is continuing to reduce test time and add some improved tests. The new tests and revised test spec is complete. The qualification of the new tests was postponed until after the first production delivery of 35 wafers was tested so as to not hold up production schedule. The qualification of the new tests was not completed in October but is continuing. Also, work is ongoing to complete the spare parts for test systems. It is expected that all will be completed by year-end.

LBNL & UCSC **Alexander A. Grillo (University Of Calif. At Santa Cruz)**

Progress was made by our CERN collaborators, in particular Francis Anghinolfi, to determine the cause of the increased power consumption after irradiation. The problem was tracked down to leakage between two n-MOS transistors which share the same p+ implant trench. Unfortunately, there are many of these structures. Further investigation by ATMEL has found no design or fabrication flaw. Most likely the problem is due to charges trapped in the oxide layer above the gap. Prior to the PRR, the power supply spec was increased to accommodate this increase in current. We are now working on a suitable screen using X-rays to guarantee a limit to the current increase with the production material.

1.1.2.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
1st ICs Avail for Prod Hybrids	4-Jan-02	--	4-Jan-02	On Schedule
10% Testing Complete	1-Feb-02	--	1-Feb-02	On Schedule
25% Testing Complete	27-Mar-02	--	27-Mar-02	On Schedule

Alexander A. Grillo (University Of Calif. At Santa Cruz)

LBNL & UCSC

ATMEL has qualified the new epitaxy subcontractor for production. We should start to receive wafers from that subcontractor in the next month. The second batch of 70 wafers was received on schedule. They arrived at UCSC for testing at month end. As yet, there are no yield results.

1.1.2.2 Hybrids/Cables/Fanouts

1.1.2.2.1 Design — Carl Haber (Lawrence Berkeley Lab.)

The hybrid design is no longer a US responsibility. The design of the MPP is complete and drawings are in the shops for fabrication.

1.1.2.2.2 Development & Prototype Fabrication — Carl Haber (Lawrence Berkeley Lab.)

A K4 series hybrid was assembled and tested acceptably. This was passed to module assembly for mounting on a detector sandwich in order to form an electrical module. The wirebonding on this hybrid, particularly for the fanouts was optimized and completed acceptably. Work was done on the process of removal of bad ABCD chips. The tooling was modified. The prototype MPP plate is in the shops for fabrication.

1.1.2.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
1st Preproduction Hybrids Avail for Mod Assy	4-Jun-01	15-Oct-01	15-Dec-01	Delayed (See #1)
Compl Preproduction Assy	13-Aug-01	21-Nov-01	21-Jan-02	Delayed (See #2)
Compl Testing of Preprod Hybrid	3-Sep-01	21-Nov-01	21-Feb-02	Delayed (See #3)
1st Prod Hybrids Avail for Mod Assy	8-Feb-02	--	8-Mar-02	Delayed (See #4)

Note #1 This will follow the hybrid design review and is set by Japanese procurement schedule. The FDR is complete but some minor mods have been circulated. We have not received word that the hybrids are available from the Japanese.

Note #2-3 Set by date of item1 above.

Note #4 Due to slips above this is shifted one month.

Carl Haber (Lawrence Berkeley Lab.)

Various discussions were held concerning availability and schedule for hybrid production. Due to potential delays in baseboards it is important to start the hybrid fabrication as early as possible. A draft startup plan was created and discussed. The first MPP plate is in fab.

1.1.2.3 Module Assembly and Test

1.1.2.3.1 Design of Assembly & Test Tooling

Milestone	Baselin	Previou	Forecas	Status

	e	s	t	
Compl Design of Preprod Mod Assy/Test	3-Sep-01	3-Nov-01	3-Feb-02	Delayed (See #1)
Module PRR	3-Sep-01	1-Mar-02	8-Mar-02	Delayed (See #2)
Compl Design of Prod Mod Assy/Test	8-Feb-02	--	8-Mar-02	Delayed (See #3)

Note #1 Now that the fixation point is settled fixtures have to be modified and tested.

Note #2 Given the delay discussed in #1 above this is the current expected date for the US module assembly PRR.

Note #3 Slipped due to 1) above.

Carl Haber (Lawrence Berkeley Lab.)

Design work is complete on the new folding fixture and the first version of the pickup tool. Parts are in the shops for fabrication. The design of the module fixation point has been agreed upon.

1.1.2.3.2 Development & Prototypes **Carl Haber (Lawrence Berkeley Lab.)**

A dummy module has been assembled successfully. It is now in metrological inspection. Metrology analysis and daq code is being modified. Additional alumina baseboards have been requested and sent to us. A baseboard support plate was built for us at RAL and is in shipment. Tests continue on the new spots recognition code. A K4 hybrid was wrapped successfully around a detector sandwich to form an electrical module. All wirebonding was completed successfully and the module functions electrically. Detailed response tests are in progress. A second electrical module is in preparation. Discussions were held concerning the use of the LBL pickup tool with the UK fixtures.

1.1.2.3.3 Production

Milestone	Baseline	Previous	Forecast	Status
Complete Preproduction Module Assembly	30-Jul-01	30-Jan-02	1-Mar-02	Delayed (See #1)
Complete Preproduction Module Testing	3-Sep-01	15-Feb-02	15-Mar-02	Delayed (See #2)
Start Full Strip Module Production	7-Jan-02	1-Mar-02	15-Mar-02	Delayed (See #3)

Note #1-2 Require pre-production hybrids which are still unavailable from Japan. Requires validation of new fixtures now that fixation point is settled.

Note #3 Defined as date of module assembly PRR.

Carl Haber (Lawrence Berkeley Lab.)

A detailed production startup plan was composed and is in discussion. Pre-production qualification will proceed now that the module fixation point is fixed.

1.1.3 ROD Design & Fabrication — Dick Jared (Lawrence Berkeley Lab.)

A defect in the VHDL code for the ROD has been found and characterized. The data from the formatter to the event fragment builder is corrupted when only 6 links in formatter 1 are active. The defect has been found to be in the masks for the event fragment builder. Preliminary test show that the defect has been corrected. The new problems have been found in the token circuitry in the formatter. The problem is understood and will be corrected in the near future. Testing is on going to find defects.

The ROD has been upgraded to the production model. The printed circuit boards (15 ea.) are in fabrication and part kits have been prepared for loading. It is expected to have the early fabrication of production model (4 ea.) completed in late October or early February. These cards will be needed for user evaluation of the ROD in the system test.

Code for the master DSP primitive that configures the front modules has been written and compiled and tested. The software works correctly except for one problem with the latency. Correction will require the use of DMA to send the data to the serial link. This will be done in the next few weeks. Testing of the serial link in the controller FPGS has shown the serial data is sent correctly to the front-end module ports. When the DMA is functional the ROD should be able to configure front-end modules. Configuration of the front-end modules is needed in the system test.

1.1.3.4 ROD Test Stand

1.1.3.4.3 SCT/Pixel Test Stand Software

Milestone	Baseline	Previous	Forecast	Status
Production Diagnostic Test Stand Completed	29-Sep-00	29-Oct-01	29-Apr-02	Delayed (See #1)

Note #1 The test stand software is completely functional for the production testing. This software will be updated for more efficiency in the next few months. The minor improvements to the software will continue till the mid part of FY 02.

1.1.3.6 ROD Prototype Evaluation

1.1.3.6.3 User Evaluation of ROD in Europe

Milestone	Baseline	Previous	Forecast	Status
SCT ATLAS Final Design Review	11-Jun-01	15-Nov-01	15-May-02	Delayed (See #1)
SCT ROD User Evaluation Complete	1-Oct-01	--	15-Apr-02	Delayed (See #2)
Pixel ATLAS Final Design Review	1-Jan-02	1-Jan-02	1-May-02	Delayed (See #3)

Note #1 The new schedule forecast a date of 4/3/02 for this review. At that time the BOC and ROD should be ready for the review.

Note #2 The complete user evaluation is predicated as completion of the production model of the BOC and ROD. The prototype TIM will be used for the testing. The limiting factor is completion of the initial

SCT DAQ. The SCT DAQ prototype is schedule to be completed in October of 2001 and the usable DAQ will be ready in January of 2002. The DAQ and cards will be used at CERN in December 2001 to early April 2002 to verify that the SCT Off Detector Electronics function as expected.

Note #3 The current new schedule predicated on user evaluation assumes the review will be late in FT 02.

1.1.3.7 ROD Production Model

1.1.3.7.1 Updating of ROD to production Model

Milestone	Baseline	Previous	Forecast	Status
SCT ATLAS ROD PRR	1-Oct-01	--	15-Nov-02	Delayed (See #1)

Note #1 The PRR is contingent on completion of the user evaluation. Please see 1.1.3.6.3 SCT ROD user evaluation complete for details.

1.1.3.7.3 Evaluation of Production Model

Milestone	Baseline	Previous	Forecast	Status
Release Production Dwg/Specs	16-May-01	--	17-Oct-01	Completed
Pixel ROD Design complete	14-Jun-01	15-Nov-01	15-Feb-02	Delayed (See #1)
Release Production Bids	4-Jul-01	--	18-Oct-01	Completed
Bid Evaluation Complete	15-Aug-01	--	19-Oct-01	Completed

Note #1 The VHDL is still under development. It is projected to be completed and evaluated by Feb 02.

1.1.3.8 ROD Fabrication

1.1.3.8.1 ROD 5% Production

Milestone	Baseline	Previous	Forecast	Status
Begin First End Cap SCT Module Ass/Test	25-Nov-01	25-Nov-02	25-Apr-02	Delayed (See #1)
Begin First Barrel SCT Module Ass/Test	27-Dec-01	27-Sep-02	27-Apr-02	Delayed (See #2)

Note #1-2 These dates are not known well because of assembly site slippage.

1.1.3.8.2 SCT ROD Production

Milestone	Baseline	Previous	Forecast	Status
ROD 45% Production complete	16-Jan-02	--	1-Oct-02	Delayed (See #1)

Note #1 The production cannot start until ATLAS has significant user evaluation and a review of the Pixel Off-detector Electronics.

1.2 TRT

Milestones with changed forecast dates:

1.2.1.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
HV Plates (Module #3) CUM #5 Available	28-Feb-01	30-Oct-01	30-Nov-01	Delayed (See #1)
CUM #32 Kit Available	31-May-01	1-Dec-02	1-Oct-01	Completed
HV Plates (Module #3) CUM #12 Available	31-May-01	31-Oct-01	31-Dec-01	Delayed (See #2)
Module Assy #2 Duke Module Assy CUM #9 Complete	31-May-01	1-Nov-01	1-Oct-01	Completed
Shells (Module #3) CUM #12 Available	31-May-01	31-Oct-01	31-Dec-01	Delayed (See #3)
CUM #37 Kit Available	29-Jun-01	29-Jun-02	29-Oct-01	Completed
HV Plates (Module #3) CUM #13 Available	29-Jun-01	29-Oct-01	29-Dec-01	Delayed (See #4)
Module Assy #2 Duke Module Assy CUM #11 Complete	29-Jun-01	29-Oct-01	29-Dec-01	Delayed (See #5)
Mangement Contingency Go-Ahead	2-Jul-01	2-Oct-01	2-Dec-01	Delayed (See #6)
Module Assy #2 Duke Module Assy CUM #13 Complete	31-Jul-01	30-Oct-01	30-Nov-01	Delayed (See #7)
Module Assy #3 Duke & IU Module Assy CUM #8 Complete	31-Jul-01	1-Nov-01	1-Dec-01	Delayed (See #8)
CUM #48 Kit Available	31-Aug-01	31-Oct-01	31-Dec-01	Delayed (See #9)
HV Plates (Module #2) CUM #19 Available	31-Aug-01	31-Oct-01	31-Dec-01	Delayed (See #10)
HV Plates (Module #3) CUM #15 Available	31-Aug-01	31-Oct-01	31-Dec-01	Delayed (See #11)
Module Assy #2 Duke Module Assy CUM #15 Complete	31-Aug-01	31-Oct-01	31-Dec-01	Delayed (See #12)
Module Assy #3 Duke & IU Module Assy CUM #10 Complete	31-Aug-01	1-Nov-01	1-Dec-01	Delayed (See #13)
CUM #25,400 Available from Hampton	28-Sep-01	28-Oct-01	28-Nov-01	Delayed (See #14)
Wire Joints -1 CUM #44 (600/m) Available	28-Sep-01	28-Oct-01	28-Dec-01	Delayed (See #15)
Module Assy #2 Duke Module Assy CUM #19 Complete	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #16)
Wire Joints -2 CUM #21 (200/m) Available	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #17)
Wire Joints -1 CUM #48 (600/m) Available	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #18)
Shells (Module #3) CUM #17 Available	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #19)
Shells (Module #2) CUM #22 Available	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #20)
Shells (Module #1) CUM #22 Available	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #21)
CUM #27,800 Available from Hampton	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #22)

Module Assy #3 Duke & IU Module Assy CUM #14 Complete	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #23)
Module Assy #1 IU Module Assy CUM #19 Complete	31-Oct-01	31-Oct-01	1-Nov-01	Delayed (See #24)
HV Plates (Module #3) CUM #17 Available	31-Oct-01	31-Oct-01	1-Nov-01	Delayed (See #25)
HV Plates (Module #2) CUM #22 Available	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #26)
HV Plates (Module #1) CUM #22 Available	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #27)
CUM #60 Kit Available	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #28)
CUM #34,843 Available from CERN	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #29)
CUM #31 Test Complete	31-Oct-01	31-Oct-01	31-Oct-02	Delayed (See #30)
Modules Production A Complete	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #31)

Note #1, 4 Waiting on HV plates.
Note #2 Delayed due to HV 3 plates.
Note #3 Shells are keeping up with production but are delayed WRT schedule.
Note #5, 7-31 Delayed.
Note #6 Delayed until October when our production rates will be clearer.

1.2.1.3 Installation

Milestone	Baseline	Previous	Forecast	Status
Installation Management Contingency Go-Ahead	2-Jul-01	2-Oct-01	2-Dec-01	See Note #1

Note #1 TBD - Project Manager together with the ATLAS Collaboration to set priorities for release of management contingency

1.2.5.1.3 Production (Qty = 64,000 + 32,000 Chips)

Milestone	Baseline	Previous	Forecast	Status
Management Contingency Go-Ahead	2-Jul-01	15-Oct-01	15-Dec-01	Delayed (See #1)

Note #1 We would have hoped that this was on schedule - sort of not entirely under our control though. - well, that was last few month's statement. The schedule is still not under our control. Right now the increased noise served in the ASDBLR00 run and now, we think, understood still leaves us somewhat uncertain about when we will actually be fully confident to go forward with pre-production and production purchases, but if the contingency go-ahead is delayed much more, then we will certainly not be able to meet the ATLAS milestones or we will have to pay much more. We were recently notified that it was necessary that the project office "be aware of the overall chip yield" prior to any consideration of release of contingency - note that this was sent to us 28 days AFTER the project office stipulated date of contingency go-ahead. The yield numbers available to us (and the project office) have not changed greatly over the last few months - still ~45% overall yield from the first wafer run - and now we have near final yields on the 00 run, better because of matching improvements (roughly 55% for he same level of cuts as the 45% for the 99 version but the confidence in any of these numbers is fairly small as the number of lots is only two. The noise question confuses this a bit, but is mostly a question of how we balance what we can live with what we are willing to change. The expectation is that one or more of the modifications

made in the recent re-run of the wafers will be fully satisfactory. The actual order will, nevertheless, have to be based on fairly conservative yield numbers or we will risk being stuck going back for additional wafers at a MUCH higher per wafer cost. Given that the cost estimates in the January 01 BCP are based on such moderately conservative yield numbers, it is highly unlikely that there would be any change in the requested (or prudent) purchase. Given that we now have evidence for some improvement in parametric yield the only plausible question remaining before Go-Ahead is whether or not the noise is fully back in a reasonable place - it is not clear that gating the Contingency release (as opposed to the actual purchase AFTER the PRR) is wise. The situation is still unchanged and so I will simply retain most of this note from last month.

1.2.1 Barrel Mechanics

1.2.1.1 Barrel Module — Ken McFarlane (Hampton University)

See details below.

1.2.1.1.1 Design — Harold Ogren (Indiana University)

Design work continues on the cooling plate, and gas and cooling the services. We completed the final drawings needed for bidding of the space frame.

1.2.1.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
HV Plates (Module #3) CUM #5 Available	28-Feb-01	30-Oct-01	30-Nov-01	Delayed (See #1)
CUM #5 Test Complete	30-Apr-01	--	30-Dec-01	Delayed (See #2)
HV Plates (Module #2) CUM #14 Available	30-Apr-01	--	30-Oct-01	Completed
CUM #32 Kit Available	31-May-01	1-Dec-02	1-Oct-01	Completed
CUM #9 Test Complete	31-May-01	--	1-Dec-01	Delayed (See #3)
HV Plates (Module #2) CUM #15 Available	31-May-01	--	1-Nov-01	Delayed (See #4)
HV Plates (Module #3) CUM #12 Available	31-May-01	31-Oct-01	31-Dec-01	Delayed (See #5)
Module Assy #2 Duke Module Assy CUM #9 Complete	31-May-01	1-Nov-01	1-Oct-01	Completed
Module Assy #3 Duke & IU Module Assy CUM #4 Complete	31-May-01	--	1-Nov-01	Delayed (See #6)
Shells (Module #3) CUM #12 Available	31-May-01	31-Oct-01	31-Dec-01	Delayed (See #7)
CUM #37 Kit Available	29-Jun-01	29-Jun-02	29-Oct-01	Completed
HV Plates (Module #2) CUM #17 Available	29-Jun-01	--	29-Nov-01	Delayed (See #8)
HV Plates (Module #3) CUM #13 Available	29-Jun-01	29-Oct-01	29-Dec-01	Delayed (See #9)
Module Assy #2 Duke Module Assy CUM #11 Complete	29-Jun-01	29-Oct-01	29-Dec-01	Delayed (See #10)
Module Assy #3 Duke & IU Module Assy	29-Jun-01	--	29-Dec-01	Delayed (See #11)

CUM #6 Complete				
Shells (Module #3) CUM #13 Available	29-Jun-01	--	29-Nov-01	Delayed (See #12)
Mangement Contingency Go-Ahead	2-Jul-01	2-Oct-01	2-Dec-01	Delayed (See #13)
CUM #27,943 Available from CERN	31-Jul-01	--	1-Oct-01	Completed
CUM #42 Kit Available	31-Jul-01	--	31-Dec-01	Delayed (See #14)
HV Plates (Module #1) CUM #18 Available	31-Jul-01	--	1-Oct-01	Completed (See #15)
HV Plates (Module #2) CUM #18 Available	31-Jul-01	--	1-Nov-01	Delayed (See #16)
HV Plates (Module #3) CUM #14 Available	31-Jul-01	--	31-Dec-01	Delayed (See #17)
Module Assy #2 Duke Module Assy CUM #13 Complete	31-Jul-01	30-Oct-01	30-Nov-01	Delayed (See #18)
Module Assy #3 Duke & IU Module Assy CUM #8 Complete	31-Jul-01	1-Nov-01	1-Dec-01	Delayed (See #19)
Shells (Module #3) CUM #14 Available	31-Jul-01	--	1-Nov-01	Delayed (See #20)
CUM #23,000 Available from Hampton	31-Aug-01	--	31-Oct-01	Completed
CUM #30,243 Available from CERN	31-Aug-01	--	31-Oct-01	Completed
CUM #48 Kit Available	31-Aug-01	31-Oct-01	31-Dec-01	Delayed (See #21)
HV Plates (Module #1) CUM #20 Available	31-Aug-01	--	31-Oct-01	Completed
HV Plates (Module #2) CUM #19 Available	31-Aug-01	31-Oct-01	31-Dec-01	Delayed (See #22)
HV Plates (Module #3) CUM #15 Available	31-Aug-01	31-Oct-01	31-Dec-01	Delayed (See #23)
Module Assy #1 IU Module Assy CUM #15 Complete	31-Aug-01	--	31-Oct-01	Completed
Module Assy #2 Duke Module Assy CUM #15 Complete	31-Aug-01	31-Oct-01	31-Dec-01	Delayed (See #24)
Module Assy #3 Duke & IU Module Assy CUM #10 Complete	31-Aug-01	1-Nov-01	1-Dec-01	Delayed (See #25)
Shells (Module #3) CUM #15 Available	31-Aug-01	--	1-Nov-01	Delayed (See #26)
CUM #25,400 Available from Hampton	28-Sep-01	28-Oct-01	28-Nov-01	Delayed (See #27)
CUM #32,543 Available from CERN	28-Sep-01	--	28-Oct-01	Completed
CUM #54 Kit Available	28-Sep-01	--	28-Nov-01	Delayed (See #28)
HV Plates (Module #1) CUM #21 Available	28-Sep-01	--	28-Nov-01	Delayed (See #29)
HV Plates (Module #2) CUM #21 Available	28-Sep-01	--	28-Nov-01	Delayed (See #30)
HV Plates (Module #3) CUM #16 Available	28-Sep-01	--	28-Dec-01	Delayed (See #31)
Module Assy #1 IU Module Assy CUM #17 Complete	28-Sep-01	--	28-Nov-01	Delayed (See #32)
Module Assy #2 Duke Module Assy CUM #17 Complete	28-Sep-01	--	28-Nov-01	Delayed (See #33)
Module Assy #3 Duke & IU Mbdule Assy CUM #12 Complete	28-Sep-01	--	28-Dec-01	Delayed (See #34)

Shells (Module #1) CUM #21 Available	28-Sep-01	--	28-Oct-01	Completed
Shells (Module #2) CUM #21 Available	28-Sep-01	--	28-Oct-01	Completed
Shells (Module #3) CUM #16 Available	28-Sep-01	--	28-Dec-01	Delayed (See #35)
Wire Joints -1 CUM #44 (600/m) Available	28-Sep-01	28-Oct-01	28-Dec-01	Delayed (See #36)
Wire Joints -2 CUM #19 (200/m) Available	28-Sep-01	--	28-Nov-01	Delayed (See #37)
CUM #25 Test Complete	30-Sep-01	--	31-May-02	Delayed (See #38)
CUM #27,800 Available from Hampton	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #39)
CUM #31 Test Complete	31-Oct-01	31-Oct-01	31-Oct-02	Delayed (See #40)
CUM #34,843 Available from CERN	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #41)
CUM #60 Kit Available	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #42)
HV Plates (Module #1) CUM #22 Available	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #43)
HV Plates (Module #2) CUM #22 Available	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #44)
HV Plates (Module #3) CUM #17 Available	31-Oct-01	31-Oct-01	1-Nov-01	Delayed (See #45)
Module Assy #1 IU Module Assy CUM #19 Complete	31-Oct-01	31-Oct-01	1-Nov-01	Delayed (See #46)
Module Assy #2 Duke Module Assy CUM #19 Complete	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #47)
Module Assy #3 Duke & IU Module Assy CUM #14 Complete	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #48)
Modules Production A Complete	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #49)
Shells (Module #1) CUM #22 Available	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #50)
Shells (Module #2) CUM #22 Available	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #51)
Shells (Module #3) CUM #17 Available	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #52)
Wire Joints -1 CUM #48 (600/m) Available	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #53)
Wire Joints -2 CUM #21 (200/m) Available	31-Oct-01	31-Oct-01	31-Dec-01	Delayed (See #54)
Wire Joints -1 CUM #100 (600/m) Available	29-Nov-01	--	29-Nov-01	Delayed (See #55)
CUM #1 Test Complete	30-Nov-01	--	30-Nov-01	Delayed (See #56)
CUM #30,100 Available from Hampton	30-Nov-01	--	30-Nov-01	Delayed (See #57)
CUM #37 Test Complete	30-Nov-01	--	30-Nov-01	Delayed (See #58)
CUM #37,143 Available from CERN	30-Nov-01	--	30-Nov-01	Delayed (See #59)
CUM #66 Kit Available	30-Nov-01	--	30-Nov-01	Delayed (See #60)
HV Plates (Module #1) CUM #24 Available	30-Nov-01	--	30-Nov-01	Delayed (See #61)
HV Plates (Module #2) CUM #23 Available	30-Nov-01	--	30-Nov-01	Delayed (See #62)
Module Assy #1 IU Module Assy CUM #21 Complete	30-Nov-01	--	30-Nov-01	Delayed (See #63)
Module Assy #2 Duke Module Assy CUM #21 Complete	30-Nov-01	--	30-Nov-01	Delayed (See #64)

Module Assy #3 Duke & IU Module Assy CUM #15 Complete	30-Nov-01	--	30-Nov-01	Delayed (See #65)
Shells (Module #1) CUM #24 Available	30-Nov-01	--	30-Nov-01	Delayed (See #66)
Shells (Module #2) CUM #23 Available	30-Nov-01	--	30-Nov-01	Delayed (See #67)
Shells (Module #3) CUM #18 Available	30-Nov-01	--	30-Nov-01	Delayed (See #68)
Wire Joints -1 CUM #52 (600/m) Available	30-Nov-01	--	30-Nov-01	Delayed (See #69)
Wire Joints -2 CUM #23 (200/m) Available	30-Nov-01	--	30-Nov-01	Delayed (See #70)
CUM #32,500 Available from Hampton	31-Dec-01	--	31-Dec-01	Delayed (See #71)
CUM #39,443 Available from CERN	31-Dec-01	--	31-Dec-01	Delayed (See #72)
CUM #43 Test Complete	31-Dec-01	--	31-Dec-01	Delayed (See #73)
CUM #71 Kit Available	31-Dec-01	--	31-Dec-01	Delayed (See #74)
HV Plates (Module #1) CUM #25 Available	31-Dec-01	--	31-Dec-01	Delayed (See #75)
HV Plates (Module #2) CUM #25 Available	31-Dec-01	--	31-Dec-01	Delayed (See #76)
HV Plates (Module #3) CUM #19 Available	31-Dec-01	--	31-Dec-01	Delayed (See #77)
Module Assy #2 Duke Module Assy CUM #22 Complete	31-Dec-01	--	31-Dec-01	Delayed (See #78)
Module Assy #3 Duke & IU Module Assy CUM #16 Complete	31-Dec-01	--	31-Dec-01	Delayed (See #79)
Shells (Module #1) CUM #25 Available	31-Dec-01	--	31-Dec-01	Delayed (See #80)
Shells (Module #2) CUM #25 Available	31-Dec-01	--	31-Dec-01	Delayed (See #81)
Shells (Module #3) CUM #19 Available	31-Dec-01	--	31-Dec-01	Delayed (See #82)
Wire Joints -1 CUM #56 (600/m) Available	31-Dec-01	--	31-Dec-01	Delayed (See #83)
Wire Joints -2 CUM #25 (200/m) Available	31-Dec-01	--	31-Dec-01	Delayed (See #84)
CUM #35,000 Available from Hampton	31-Jan-02	--	31-Jan-02	Delayed (See #85)
CUM #41,743 Available from CERN	31-Jan-02	--	31-Jan-02	Delayed (See #86)
CUM #49 Test Complete	31-Jan-02	--	31-Jan-02	Delayed (See #87)
CUM #75 Kit Available	31-Jan-02	--	31-Jan-02	Delayed (See #88)
HV Plates (Module #1) CUM #26 Available	31-Jan-02	--	31-Jan-02	On Schedule
HV Plates (Module #2) CUM #26 Available	31-Jan-02	--	31-Jan-02	On Schedule
HV Plates (Module #3) CUM #20 Available	31-Jan-02	--	31-Jan-02	On Schedule
Module Assy #1 IU Module Assy CUM #24 Complete	31-Jan-02	--	31-Jan-02	On Schedule
Module Assy #2 Duke Module Assy CUM #24 Complete	31-Jan-02	--	31-Jan-02	On Schedule
Module Assy #3 Duke & IU Module Assy CUM #17 Complete	31-Jan-02	--	31-Jan-02	On Schedule
Shells (Module #1) CUM #26 Available	31-Jan-02	--	31-Jan-02	On Schedule

Shells (Module #2) CUM #26 Available	31-Jan-02	--	31-Jan-02	On Schedule
Shells (Module #3) CUM #20 Available	31-Jan-02	--	31-Jan-02	On Schedule
Wire Joints -1 CUM #60 (600/m) Available	31-Jan-02	--	31-Jan-02	On Schedule
Wire Joints -2 CUM #27 (200/m) Available	31-Jan-02	--	31-Jan-02	On Schedule
CUM #37,250 Available from Hampton	28-Feb-02	--	28-Feb-02	On Schedule
CUM #44,043 Available from CERN	28-Feb-02	--	28-Feb-02	On Schedule
CUM #55 Test Complete	28-Feb-02	--	28-Feb-02	On Schedule
CUM #79 Kit Available	28-Feb-02	--	28-Feb-02	On Schedule
HV Plates (Module #1) CUM #28 Available	28-Feb-02	--	28-Feb-02	On Schedule
HV Plates (Module #2) CUM #27 Available	28-Feb-02	--	28-Feb-02	On Schedule
HV Plates (Module #3) CUM #21 Available	28-Feb-02	--	28-Feb-02	On Schedule
Module Assy #1 IU Module Assy CUM #25 Complete	28-Feb-02	--	28-Feb-02	On Schedule
Module Assy #2 Duke Module Assy CUM #25 Complete	28-Feb-02	--	28-Feb-02	On Schedule
Module Assy #3 Duke & IU Module Assy CUM #18 Complete	28-Feb-02	--	28-Feb-02	On Schedule
Module Assy #3 Duke & IU Module Assy CUM #34 Complete	28-Feb-02	--	28-Feb-02	On Schedule
Shells (Module #1) CUM #28 Available	28-Feb-02	--	28-Feb-02	On Schedule
Shells (Module #2) CUM #27 Available	28-Feb-02	--	28-Feb-02	On Schedule
Shells (Module #3) CUM #21 Available	28-Feb-02	--	28-Feb-02	On Schedule
Wire Joints -1 CUM #64 (600/m) Available	28-Feb-02	--	28-Feb-02	On Schedule
Wire Joints -2 CUM #29 (200/m) Available	28-Feb-02	--	28-Feb-02	On Schedule
CUM #40,000 Available from Hampton	29-Mar-02	--	29-Mar-02	On Schedule
CUM #63 Test Complete	29-Mar-02	--	29-Mar-02	On Schedule
CUM #82 Kit Available	29-Mar-02	--	29-Mar-02	On Schedule
HV Plates (Module #1) CUM #29 Available	29-Mar-02	--	29-Mar-02	On Schedule
HV Plates (Module #2) CUM #29 Available	29-Mar-02	--	29-Mar-02	On Schedule
HV Plates (Module #3) CUM #22 Available	29-Mar-02	--	29-Mar-02	On Schedule
Module Assy #1 IU Module Assy CUM #26 Complete	29-Mar-02	--	29-Mar-02	On Schedule
Module Assy #2 Duke Module Assy CUM #26 Complete	29-Mar-02	--	29-Mar-02	On Schedule
Module Assy #3 Duke & IU Module Assy CUM #19 Complete	29-Mar-02	--	29-Mar-02	On Schedule
Shells (Module #1) CUM #29 Available	29-Mar-02	--	29-Mar-02	On Schedule

Shells (Module #2) CUM #29 Available	29-Mar-02	--	29-Mar-02	On Schedule
Shells (Module #3) CUM #22 Available	29-Mar-02	--	29-Mar-02	On Schedule
Wire Joints -1 CUM #68 (600/m) Available	29-Mar-02	--	29-Mar-02	On Schedule
Wire Joints -2 CUM #31 (200/m) Available	29-Mar-02	--	29-Mar-02	On Schedule
CUM #46,343 Available from CERN	31-Mar-02	--	31-Mar-02	On Schedule

Note #1 Waiting on HV plates.

Note #2 Testing at Hampton still not operational.

Note #3-4, 6 Delayed due to pause.

Note #5, 9, 11 Delayed due to HV 3 plates.

Note #7 Shells are keeping up with production but are delayed WRT schedule.

Note #8, 10, 12, 14-37, 39-88 Delayed.

Note #13 Delayed until October when our production rates will be clearer.

Seog Oh (Duke University)

Wire Joint Aging Study

Unexpectedly the aging test chamber stopped holding the HV after ~two weeks. We traced the problem to a straw and disabled it to continue the test. However, another channel died the following day. We decided to investigate and found that the wire joints were failing. It seemed that glass bead were being etched away (possibly by fluorine radicals). This is a very serious problem. We notified the TRT collaborators and mapped the strategy. First was that we do the same test without CF_4. The second was to look for a replacement for the glass wire joints. We are putting all our resources to understand the problem and find a solution.

HV Plates

The HV plate procurement is moving well. We have received all Type I plates. The rest of Type II and type III plates are being machined and assembled.

Module Construction Status

Type 2.10 : Stringing is finished and going through the final tests.

Type 2.11 : Stringing is finished and going through the final tests.

Due to the aging problem, we have stopped the module construction, including the mechanical construction. We will resume the mechanical construction in November.

Wire-joint production: The wire joint production has stopped until the aging problem is addressed.

Ken McFarlane (Hampton University)

Production Tooling: A new gluing workstation was put in operation to process HV/TP plate kits.

Staff

We now have a total of 6 technicians (including the QA tech, who now does assembly work on tension plates and capacitor barrels, and works on the Module Test Stand). This number appears optimal for the current set of production tasks. (There will be changes in November, and we will need to re-optimize for that.)

1.2.1.1.3.1 Detector Elements

1.2.1.1.3.1.1 Straws: A shipment of straws arrived from PNPI.

1.2.1.1.3.1.1.2 End sockets (end plugs)

1.2.1.1.3.1.1.4.1 Twister

1.2.1.1.3.1.1.4.2 Twister

1.2.1.1.3.1.1.8.2 Wire bushing (eyelet)

1.2.1.1.3.1.1.8.3 Crimp pin (taper pin)

1.2.1.1.3.1.1.8.5, 6 Gas connections

All purchase orders or contracts for the above components have been placed, and deliveries are on schedule. An order for new gas connections is being placed, to improve performance.

1.2.1.1.3.4 Assembly

Straw subassemblies: Production continued with no special difficulties. A record number of straws (2,773) was processed in October (compared with a target of 2,668).

Radiator packs: Production continued with no special difficulties.

Dividers: Production continued with no special difficulties.

Wire supports: Production continued with no special difficulties.

Capacitor Barrels: Produced as needed for tension-plate processing.

Tension plates: These are now processed as needed to create HV plate/TP kits. HV plate testing and assembly with tension plates. Production continued with no special difficulties.

Capacitor Assembly: No activity this month. The final decision on capacitor type has not been made.

1.2.1.1.3.1.1.8.5, 6 Gas connections

Active gas fittings are produced as needed for TP/HV kits.

Harold Ogren (Indiana University)

Shells

Vison Composites has increased their production of "in-spec" shells. This was in large due to a very successful run of shells on a new roll of prepreg. They now think that the earlier failures were do to some effect of the prepreg which they will not monitor carefully. Their goal is to deliver about 6 modules a month. They will be waiting for material in November, but hope to make up production with reworked modules during this period.

Dividers

We will have to make some additional type 1 dividers, since Hampton has notified us that they are short on materials. It appears that many were used for earlier prototypes, when the assembly techniques were being worked out. We have contacted the local machine shop that produced the original dividers. The material- Ultem is on order and should be here in November. Assuming we can get the pieces finished in December, this will not hold up the schedule.

Modules

Module production began at a planned pace with two type 1 modules completed and a module type 3 in assembly, but the wire joint failure in the middle of the month stopped all wire stringing. Two modules are now waiting for stringing. We are continuing with the mechanical side of production, that is, completion of the module up to the point of stringing, including the first pressure test and fitting of the tension plates.

After several confirming tests, we have concluded that the glass wire joint cannot be operated in the standard mixture of Xe-CF_4-CO_2 at high radiation. This is a considerable setback. We are developing several alternatives. One is a change of gas mixture which would allow us to use the present glass wire joints, the other, the design and production of a new type wire joint that will be not destroyed during high radiation operation of the chamber. Both paths will require extensive testing, but the change of gas for both barrel and endcaps would also require aging tests for both systems.

We are preparing to move one of the stringing stations from Indiana to Hampton and to move the radiator assembly from Hampton to Indiana. This will allow us to keep the present staff fully occupied, and to begin to build up a capability at Hampton for wire stringing when we can resume.

1.2.1.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
Production Management Contingency Go-Ahead	2-Jul-01	--	2-Dec-01	See Note #1

Note #1 TBD - Project Manager together with the ATLAS Collaboration to set priorities for release of management contingency.

1.2.1.3 Installation

Milestone	Baseline	Previous	Forecast	Status
Installation Management Contingency Go-Ahead	2-Jul-01	2-Oct-01	2-Dec-01	See Note #1

Note #1 TBD - Project Manager together with the ATLAS Collaboration to set priorities for release of management contingency

1.2.5 TRT Electronics

1.2.5.1 ASD/BLR

1.2.5.1.1 Design **Richard Van Berg (University of Pennsylvania)**

No new ASDBLR design work. We are waiting for the wafers from DMILL with the metal changes mentioned last month to check noise and input protection properties - expected to arrive first of November.

1.2.5.1.2 Prototype

Milestone	Baseline	Previous	Forecast	Status
ASDBLR Design Frozen	13-Jul-01	--	15-Nov-01	Delayed (See #1)
Production Readiness Review	11-Jan-02	--	11-Jan-02	Delayed (See #2)
Start Production	18-Jan-02	--	18-Jan-02	Delayed (See #3)

Note #1 The new "properly processed" wafers arrived in mid July and plastic packaged parts were delivered on the 31st. Preliminary measurements indicate that matching and other functionality is as expected (hoped), however, the noise measurements are not as good as the SPice simulations would have indicated. We now believe we understand the cause of this discrepancy and have submitted metalization changes to ATMEL that should clear up the effect. Those wafers should be available in early November and so it is possible that we would be able to settle on a final configuration in mid November. This note from last month is still the case.

Note #2 Based on getting noise and input protection information from the remetalled wafers in mid November plus completing all other tests and people availability will put a PRR (or whatever we call it) in mid January or somewhat later - final date will be set after first round measurements.

Note #3 Production could (and should) start ASAP after the PRR in early 02. This is dependent on the review and availability of full funding.

Richard Van Berg (University of Pennsylvania)

A few further tests on the ASDBLR00 noise performance, especially after the laser cut modification of a single chip, confirm our initial impression that the increased noise is due to an error in estimating (extracting) the capacitance associated with the input protection network. ATMEL has finished processing the new wafers (we will get seven) and we received them in early Nov. Four wafers have been shipped to our packager(s) to be put in TQFP packages. Those devices should be back by the third week in November at which point we get to learn which of the variations in input protection is optimal in terms of noise/protection trade off. Unless there are further surprises that should allow us to freeze the ASDBLR design and prepare for a design review (PRR or whatever one wishes to call it) in early 2002 (probably end of January or mid February - driven mostly by the availability of reviewers and time to fully document the tests both of noise questions and test beam and radiation results.

1.2.5.1.3 Production (Qty = 64,000 + 32,000 Chips)

Milestone	Baseline	Previous	Forecast	Status
Management Contingency Go-Ahead	2-Jul-01	15-Oct-01	15-Dec-01	Delayed (See #1)

Note #1 We would have hoped that this was on schedule - sort of not entirely under our control though. - Well, that was last few month's statement. The schedule is still not under our control. Right now the increased noise served in the ASDBLR00 run and now, we think, understood still leaves us somewhat uncertain about when we will actually be fully confident to go forward with pre-production and production purchases, but if the contingency go-ahead is delayed much more, then we will certainly not be able to meet the ATLAS milestones or we will have to pay much more. We were recently notified that it was necessary that the project office "be aware of the overall chip yield" prior to any consideration of release of contingency - note that this was sent to us 28 days AFTER the project office stipulated date of contingency go-ahead. The yield numbers available to us (and the project office) have not changed greatly over the last few months - still ~45% overall yield from the first wafer run - and now we have near final yields on the 00 run, better because of matching improvements (roughly 55% for he same level of cuts as the 45% for the 99 version but the confidence in any of these numbers is fairly small as the number of lots is only two. The noise question confuses this a bit, but is mostly a question of how we balance what we can live with what we are willing to change. The expectation is that one or more of the modifications made in the recent re-run of the wafers will be fully satisfactory. The actual order will, nevertheless, have to be based on fairly conservative yield numbers or we will risk being stuck going back for additional wafers at a MUCH higher per wafer cost. Given that the cost estimates in the January 01 BCP are based on such moderately conservative yield numbers, it is highly unlikely that there would be any change in the requested (or prudent) purchase. Given that we now have evidence for some improvement in parametric yield the only plausible question remaining before Go-Ahead is whether or not the noise is fully back in a reasonable place - it is not clear that gating the Contingency release (as opposed to the actual purchase AFTER the PRR) is wise. The situation is still unchanged and so I will simply retain most of this note from last month.

Richard Van Berg (University of Pennsylvania)

Not yet, but closing. We hope to be able to submit the PO (or first of the required series - how do we want to stage the purchase and when will we have authority to commit all the funds for full production?) for production soon after the PRR in Jan or Feb 2002 in order to capitalize on ATMEL's present focus on DMILL and the concomitant expected high yields and the incidental availability of foundry capacity. This should be independent of DTMROC questions.

1.2.5.2 DTM/ROC

1.2.5.2.1 Design — Richard Van Berg (University of Pennsylvania)

All DTMROC design effort is concentrated on the DSM version. We believe that all blocks are complete and verified, that the tools exist to verify the complete design, and that we are ready for a final design review. This review has been scheduled for Nov. 15 and we even hope to have most of the review documents complete by Nov. 8th (but not all unfortunately - would be nice to break with tradition). At the last TRT meeting in CERN in Oct. it was proposed that we add in temperature and voltage measurement capability to the design - this opens the possibility of reducing the services cable plant in the ID and giving

us much finer grained monitoring of the operating environment. The extra circuitry required is minimal and the only new cells (a precision comarator and a diode) have already been designed and verified.

1.2.5.2.2 Prototype **Richard Van Berg (University of Pennsylvania)**

Beam and bench tests of the End Cap boards at CERN with 00 silicon have continued to demonstrate that the basic design more than meets our requirements. Similar progress has not yet been made in the case of the Barrel because of the lack of a low noise implementation of the board set but this could change by New Years.

Signetics Korea has now closed the loop with respect to FBGA packaging for both the ASDBLR and the DTMROC. The substrated design is proceeding and they should be ready for wafers in early to mid Dec. We have reserved three wafers of 00 and three wafers of 01 (the ASDBLR remetalization run) silicon for FBGA packages.

1.2.5.3.1 Design **Richard Van Berg (University of Pennsylvania)**

The end cap triple flex and ASDBLR board designs are being modified at CERN to take the 00 silicon for system and radiation tests. This has taken somewhat longer than expected due to some confusion about requirements - we hope that new boards will be available for tests in December. Note that the changes are minor and some testing has been completed by using manual mods of the old boards.

1.2.5.3.2 Prototype **Richard Van Berg (University of Pennsylvania)**

The test beam in Sept/Oct has operated two sets of triple flex boards on two sector prototypes (768 channels) more or less successfully (there were some noise problems which was to be expected because we do not have a realistic Faraday cage or some of the other expected final design prophylactic measures in place).

1.2.5.4 Common Electronics **Richard Van Berg (University of Pennsylvania)**

A small amount of design work has gone forward on the proposed bulk HV system, but we are not yet to the point of having a design to construct.

1.2.5.5 Beam Test

Milestone	Baseline	Previous	Forecast	Status
End of 01 Test Beam	28-Sep-01	--	4-Nov-01	Delayed (See #1)

Note #1 We have been granted additional time up through Nov. 4 01.

Richard Van Berg (University of Pennsylvania)

The 2001 beam test ended on 4 November with indications that we achieved most of our goals. Detailed analysis of the acquired data will provide the actual answers. However, the DAQ operated (not without a few "Perils of Pauline") well and the high rate ASDBLR00 tests also were completed with no problems. Now we get to look at the data and plan what the program should and could be for 2002.

1.2.5.6 System Integration & Installation

Milestone	Baseline	Previous	Forecast	Status
System Design Certified	1-Oct-01	--	1-Jan-02	Delayed (See #1)

Note #1 There are really two different systems - the End Cap where we have made great progress, but probably need to have one more round of tests using the 00 (i.e. "final") level silicon. This is waiting on CERN to finish the minor revisions to the boards and so is probably likely around the new year. For the Barrel we have not yet really gotten a viable full design so that must be achieved prior to being able to "certify" it. That process will surely take us beyond the first of the year, but new stamp boards and FBGA packages should be available to start first serious testing at about the new year.

Richard Van Berg (University of Pennsylvania)

We have made some progress on Barrel testing, have mapped out the response of our (noisy) flex boards along a snake cable and, at the digital level, demonstrated good performance - the snake cable seems to work well as a data transmission medium - we have not yet tested power distribution or mechanical fit issues (this effort and Test Beam require the same resources and since Oct was Test Beam we made only modest progress in SI&I). We have worked extensively with Lund in developing the design for a non-flex FBGA based three (or two) layer postage stamp design. This design is now well advanced and should be available as a completed printed circuit prior to delivery of actual FBGA devices. That will be a critical set of tests - can we achieve the required noise performance within the space constraints imposed by the mechanics?

1.3 ARGON

Milestones with changed forecast dates:

1.3.2.2.4 Installation

Milestone	Baseline	Previous	Forecast	Status
Ship End-Cap C to CERN	5-Mar-01	20-Oct-01	20-Feb-02	Delayed (See #1)
Installation HVFT ports on Endcap C	5-Sep-01	25-Nov-01	25-Mar-02	Delayed (See #2)
Barrel Install Complete	1-Nov-01	20-Jan-02	20-Mar-02	Delayed (See #3)
Installation HVFT on Endcap C Complete (mechanical)	1-Nov-01	20-Jan-02	20-Mar-02	Delayed (See #4)
Ship End-Cap A to CERN	1-Feb-02	1-Feb-02	1-Mar-02	Delayed (See #5)
Installation HVFT on Endcap C Complete (Cables)	20-Feb-02	20-Jan-02	20-Apr-02	Delayed (See #6)
Install HVFT on Endcap A Complete (mechanical)	28-Feb-02	28-Feb-02	28-Mar-02	Delayed (See #7)
Install HVFT on Endcap A Complete (Cables)	28-Feb-02	28-Feb-02	28-Apr-02	Delayed (See #8)

Note #1 Shipment combined with signal FT.
Note #2, 4-5, 7-8 Delay will match the cryostat availability.
Note #3-4, 6 The order of installation of HV and signal FT has been changed. HV cables will be installed after completion of signal FT installation.

1.3.3.2.2 Quality Meter Prototype

Milestone	Baseline	Previous	Forecast	Status
Specification PRR Review	1-Aug-01	15-Dec-01	31-Oct-01	Completed (See #1)

Note #1 It has been agreed between BNL and CERN that the content of meetings at BNL and CERN, plus E Mail communications and WWW distributed information satisfy the requirements and serve as the Production Readiness Review.

1.3.6.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Start EC Pedestal Delivery to CERN	31-Dec-01	31-Dec-01	1-Mar-02	Delayed (See #1)
Start Barrel Pedestal Delivery to CERN	31-Dec-01	31-Dec-01	1-Mar-02	Delayed (See #2)

Note #1-2 Delay matches installation schedule.

1.3.7.1.2 Pre-Proto/Mod 0/Atlas Prototype

Milestone	Baseline	Previous	Forecast	Status
Final Dec. DMILL/IBM	7-Dec-01	7-Dec-01	15-Oct-01	Completed

1.3.8.2.1 Design/Electronic Tooling/Comp. Specs

Milestone	Baseline	Previous	Forecast	Status
Circuit Design of ATLAS receiver Complete	12-Aug-01	16-Nov-01	30-Jan-02	Delayed (See #1)
Final Design Complete	4-Oct-01	30-Jan-02	30-Mar-02	Delayed (See #2)
Critical Design Review	12-Dec-01	30-Mar-02	30-May-02	Delayed (See #3)

Note #1 The investigation of a lower noise solution to the variable gain amplifier in the receiver signal chain has led to a delay of about 6 months in the design of the system.
Note #2 It is likely that this milestone will be missed by a few months, due to the delay arising from the study of the variable gain amplifier mentioned above.
Note #3 This milestone has slipped, since the production of the prototype module is delayed.

1.3.8.2.3 Production (Qty - 187 Boards)

Milestone	Baseline	Previous	Forecast	Status
Production Readiness Review	4-Mar-02	4-Mar-02	4-Oct-02	Delayed (See #1)
Start Production	4-Mar-02	4-Mar-02	4-Nov-02	Delayed (See #2)
PM Appr of RCV/Mon Bds Purch Req.'s	18-Mar-02	18-Mar-02	18-Nov-02	Delayed (See #3)

Note #1 The Receiver system design has been delayed by about 1 year as discussed above. The design review should be held at the end of 01, and we anticipate holding the PRR in Oct of 02.
Note #2 We will start production once the bid has been selected.
Note #3 We anticipate approval of the PM to proceed with production shortly after the PRR.

1.3.10.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
FCAL1-C Interconnects Complete	30-Apr-01	30-Nov-01	30-Dec-01	Delayed (See #1)

Note #1 We decided to send out only half of the interconnect boards to have the sockets installed. This is to provide better QC and to encourage low pricing. This will delay completion a bit but not seriously.

1.3.10.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
PCBs received at AZ	21-Nov-00	15-Dec-01	31-Jan-02	Delayed (See #1)

Note #1 Revision A of the board is stuffed and is being tested. There will be a Revision B to correct a few flaws. The board production should be completed soon thereafter.

1.3.1 Barrel Cryostat

1.3.1.5 Assembly & Test in West Hall

Milestone	Baseline	Previous	Forecast	Status
Final Kryostat Acceptance (KHI-CERN)	31-Aug-01	--	15-Feb-02	Delayed (See #1)
Calorimeter Support Structure Complete	31-Oct-01	--	31-Oct-01	Completed

Note #1 Provisional acceptance and transfer of ownership to CERN completed. Final acceptance awaits completion of chimney weld repair.

Barrel Cryostat Report **Jack Sondericker (Brookhaven National Lab.)**

As the feedthroughs are being installed in the Outer Cold Vessel of the cryostat, the saga of the repair of the chimney crack continues. The welding plan mentioned in last month's report is a result of finding a possible solution that will be acceptable to all parties, CERN, BNL and Kawasaki. The plan proposed is to remove a few millimeters of crack surface and "butter over" the crack with weld to make it vacuum tight. We were close to agreement during the beginning of the month, waiting for a positive indication from TIS, CERN's technical Inspection and Safety Division when it was discovered that the ANSYS modeling contained an error. The chimney wall thickness shown as 30mm was in fact 20 mm.

During the last of the month the chimney analysis was rerun using the reduced wall thickness. Results of the simulated crack area stresses showed a reduction in magnitude from the previous 30 mm case because of the increased flexure afforded by the thinner wall. Results are under review by CERN TIS; just about where we were one month ago.

1.3.2 Feedthrough

1.3.2.1 FT-Signal

1.3.2.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Last Pin Carrier Delivery	1-Mar-01	--	1-Feb-02	Delayed (See #1)
34 FT Complete	15-Oct-01	--	15-Oct-01	Completed
54 FT Complete	17-Dec-01	--	17-Dec-01	On Schedule
Production Complete (68)	15-Feb-02	--	15-Feb-02	On Schedule

Note #1 After initial delay, the production matches the new ATLAS schedule

Bob Hackenburg (Brookhaven National Lab.)

In October, FT production hit number 40, with 20 FTs having been shipped to CERN. Pin carrier production and all other components of the project remain in good shape, and there are no problems to report.

1.3.2.1.4 Installation

Milestone	Baseline	Previous	Forecast	Status
Installation	17-Jan-01	--	30-Sep-02	Delayed (See #1)
Last Shipment	31-Oct-01	--	30-Aug-02	Delayed (See #2)

Note #1 The completion date matches new ATLAS schedule.

Note #2 The last shipment date matches the new ATLAS schedule. Feedthroughs production will be completed earlier.

Bob Hackenburg (Brookhaven National Lab.)

In October, 16 FTs were successfully installed on the barrel cryostat, with many of them leak checked (good) and two random FTs fully tested electrically, both good. The balance of the 20 FTs already shipped to CERN from BNL, plus 8 more FTs just shipped, should be installed in November.

1.3.2.2 HV Feedthrough

1.3.2.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
2 Complete HV Feedthrough Ports	1-Mar-01	--	20-Jan-02	Delayed (See #1)
Barrel FTs (Electrical) delivered to CERN	1-Jun-01	--	15-Feb-02	Delayed (See #2)
Production Complete	14-Sep-01	--	20-Jan-02	Delayed (See #3)

Note #1, 3 The order of installation of HV and signal FT has been changed. HV cables will be installed after completion of signal FT installation.

Note #2 The delivery will match the installation program.

Michal Rijssenbeek (SUNY Stony Brook)

1.3.2.2.3.1 Warm Connectors

REDEL/LEMO warm connectors are in house. The first HVFT plate had finished, but has to be redone because of changes in EMB requirements for cabling (see below).

1.3.2.2.3.2 Cold Connectors: Cold connectors are in house.

1.3.2.2.3.3 HV Wire: Task Finished.

1.3.2.2.3.6 Sealed Wire FT (WFT): Task Finished.

1.3.2.2.3.4-5 Filter Modules and Filter Crate

All HV parts have been delivered. Filter daughter boards are in house. Front panels from Rittal were rejected because of poor quality. New panels have been made in the Stony Brook department machine shop.

1.3.2.2.3.7-9 Vacuum Components for the High Voltage Feedthrough (HVFT)

All eight HVFTs have been welded and tested at BNL. That finishes all HVFT mechanical/cryogenic work. One HVFT was shipped to CERN in mid-August, and has been installed on Oct 10. The second barrel FT is prepared for shipping to CERN.

1.3.2.2.3.10 Assembly

The EM Calorimeter builders requested that one spare wire be included in each 7-wire HV bundle, in order to provide separate HV supply for sick calorimeter cells found during calorimeter module testing. This caused a re-mapping of the HV connection diagram, and subsequent rebundling of the HV wires. This rebundling is now starting. After completion of the warm connector side, cold connectors will be installed. Then, a final HV and leak test will be done, using the actual feedthrough. At that time the bundle insertion procedure will be tested as well.

1.3.2.2.4 Installation

Milestone	Baseline	Previous	Forecast	Status
Ship End-Cap C to CERN	5-Mar-01	20-Oct-01	20-Feb-02	Delayed (See #1)
Installation HVFT ports on Endcap C	5-Sep-01	25-Nov-01	25-Mar-02	Delayed (See #2)
Barrel Install Complete	1-Nov-01	20-Jan-02	20-Mar-02	Delayed (See #3)
Installation HVFT on Endcap C complete (mechanical)	1-Nov-01	20-Jan-02	20-Mar-02	Delayed (See #4)
Ship End-Cap A to CERN	1-Feb-02	1-Feb-02	1-Mar-02	Delayed (See #5)
Installation HVFT on Endcap C complete (Cables)	20-Feb-02	20-Jan-02	20-Apr-02	Delayed (See #6)
Install HVFT on Endcap A complete (Cables)	28-Feb-02	28-Feb-02	28-Apr-02	Delayed (See #7)
Install HVFT on Endcap A complete (mechanical)	28-Feb-02	28-Feb-02	28-Mar-02	Delayed (See #8)

Note #1 Shipment combined with signal FT.

Note #2, 4-5, 7-8 Delay will match the cryostat availability.

Note #3, 4, 6 The order of installation of HV and signal FT has been changed. HV cables will be installed after completion of signal FT installation.

Note #6 The order of installation of HV and signal FT has been changed. HV cables will be installed after completion of signal FT installation

Michal Rijssenbeek (SUNY Stony Brook)

One HVFT was shipped to CERN in mid-August, and has been installed on Oct 10. The second barrel HVFT is prepared for shipping to CERN. Tefzel cable mounts, tefzel cable ties, and M5 SS bolts are at CERN and available for cable routing. We will install the HV cable tree and do the HV wire routing when all welding has finished, and after cleaning of the cryostat (i.e. with the signal FT cables in place). This second phase of installation is foreseen for January/March 2002.

1.3.3 LAr Cryogenics

1.3.3.1 LN2 Refrigerator System

1.3.3.1.2 LN2 Ref. System Procurement

Milestone	Baseline	Previous	Forecast	Status
Start Production	1-Aug-01	--	15-Sep-01	Completed

Jack Sondericker (Brookhaven National Lab.)

Atlas Nitrogen Refrigerator System Procurement has been completed. Fabrication commenced end of September 2001

1.3.3.1.3 LN2 Ref. System Fabrication

Milestone	Baseline	Previous	Forecast	Status
Ln2 Ref. System Fabrication	1-Jun-01	--	1-Sep-03	Delayed (See #1)
LN2 Ref. System Fabrication Start	1-Jun-01	--	15-Sep-01	Completed

Note #1 The completion date of system installation matches new ATLAS installation schedule.

Jack Sondericker (Brookhaven National Lab.)

While attending LAr Week, which commenced on October 8th, a representative of the ATLAS Nitrogen Refrigerator System arranged to have a kick off meeting with Air Liquide at a convenient location, CERN. Members of the ATLAS detector Cryogenics Group were present as the third interested party, the eventual owners of the system. Project teams were presented, updated planning was discussed, reviewed possible suppliers, and settled on an ANRS Production Readiness Review in December 2001.

A few technical questions were asked of us; some answered while others pertained to real estate questions to be answered by representatives of CERN. Meanwhile, Air Liquide is busy specifying and ordering major ANRS equipment to satisfy the first project milestone so that they can be eligible for the first payment of 30% of the total project cost.

1.3.3.1.4 Installation @ Testing CERN

Milestone	Baseline	Previous	Forecast	Status
Installation @ Testing CERN	1-Mar-02	--	1-Oct-03	Delayed (See #1)
Installation @ Testing CERN Start	1-Mar-02	--	1-Mar-02	On Schedule

Note #1 The completion date matches new ATLAS schedule.

1.3.3.2 LN2 Quality Meter System

1.3.3.2.2 Quality Meter Prototype

Milestone	Baseline	Previous	Forecast	Status
Quality Meter Prototype	1-May-00	--	21-Sep-01	Completed
Specification PRR Review	1-Aug-01	15-Dec-01	31-Oct-01	Completed (See #1)

Note #1 It has been agreed between BNL and CERN that the content of meetings at BNL and CERN, plus E Mail communications and WWW distributed information satisfy the requirements and serve as the Production Readiness Review.

Quality Meter Prototype **Jack Sondericker (Brookhaven National Lab.)**

During the month the prototype Quality meter was pneumatically pressure tested again to beyond the 25 bar requirements of CERN TIS. Additional cold runs were carried out to check repeatability of the sensor and electronics. No problems were found.

It has been agreed with CERN that there is no need for a formal Production Readiness Review in that meetings were held at BNL last May and at CERN in July and during this month. In addition, throughout this time frame, information was also distributed by E Mail and summarized at WWW site-

http://www.agsrhichome.bnl.gov/RHIC/Cryogroup/index.htm.

Development and prototyping of the Quality Mater has been completed.

1.3.3.2.3 Quality Meter Production

Milestone	Baseline	Previous	Forecast	Status
Parts and Material Start	29-Aug-01	--	15-Jan-02	Delayed (See #1)
Quality Meter Production	1-Oct-01	--	30-Jun-02	Delayed (See #2)
Assembly Start	26-Dec-01	--	26-Jun-02	Delayed (See #3)
Machining and Welding Start	26-Dec-01	--	26-Jun-02	Delayed (See #4)
Tests and calibration Start	26-Dec-01	--	26-Dec-02	Delayed (See #5)
Parts and Material Complete	28-Dec-01	--	28-Aug-02	Delayed (See #6)

Note #1, 3-6 Delay matches the new ATLAS schedule. Not on critical path.

Note #2 Delay matches the new ATLAS schedule.

1.3.4 EM Electronics/MB System

1.3.4.1 Readout Electronics

1.3.4.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Indust. Purchase Last Delivery	1-Mar-02	--	1-Mar-02	On Schedule

1.3.4.2 Motherboard System

1.3.4.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
Delivery of Batch 11 boards	1-Nov-01	[New]	30-Oct-01	Completed (See #1)
Delivery of Batch 12 boards	1-Nov-01	[New]	30-Oct-01	Completed (See #2)
Last Delivery of SB & MB PC Boards	1-Dec-01	--	1-Nov-02	Delayed (See #3)
Shipment of Batch 13 boards	1-Dec-01	[New]	1-Dec-01	On Schedule
50% MB System Production Complete	2-Dec-01	--	2-Dec-01	On Schedule
Shipment of Batch 14 boards	15-Dec-01	[New]	15-Dec-01	On Schedule

Note #1 Shipped to CERN on October 24, 2001.

Note #2 Shipped to Saclay on Nov. 1, 2001.

Note #3 Matches the module construction schedule.

Srini Rajagopalan (Brookhaven National Lab.)

Batch 3: completed, packed, shipped to Saclay on May 3, 2001

Batch 4: completed, packed, shipped to Annecy on May 6, 2001

Batch 5: completed, packed, shipped to Saclay on May 31, 2001

Batch 6: completed, packed, shipped to Annecy on July 11, 2001

Batch 7: completed, packed, shipped to Annecy on August 24, 2001

Batch 8: completed, packed, shipped to CERN on August 24, 2001

Batch 9: completed, packed, shipped to Saclay on September 4, 2001

Batch 10: completed, packed, shipped to Annecy on September 21, 2001

Batch 11: completed, packed, shipped to CERN on October 24, 2001

Batch 12: completed, packed, shipped to Saclay on November 1, 2001

For batch #13: Target date for shipment to Annecy is November 27, 2001

Summing Boards: All boards received, and being tested.

High Voltage Board: All boards received, and being tested.

Front Motherboards: All boards received, and being tested.

Back Motherboards: All boards received, and being tested.

Alignment Boards: All boards received, and tested.

For Batch #14 Target date for shipment is December 4, 2001

Summing Boards: All boards received, and being inspected.

High Voltage Board: All Boards received, inspected and in test.

Front Motherboards: All boards received, inspected, and in test.

Back Motherboards: All boards received, inspected, and in test.

Alignment Boards: In BNL stock.

1.3.5 Pre amp/Calibration

1.3.5.1 Preamps

1.3.5.1.3 Production (QTY=30000)

Milestone	Baseline	Previous	Forecast	Status
Start Preamp Deliveries to FEB	3-Sep-01	--	1-Apr-02	Delayed (See #1)
Final Production Complete	29-Mar-02	--	29-Mar-02	On Schedule

Note #1 BNL is holding completed Preamps until FEB requests them. To date, 38% of all preamps have been completely tested and are ready for shipment.

Hong Ma (Brookhaven National Lab.)

IO-826: received none from vendor since last report. All have been tested.

Total: 3087 have been completed and ready for shipment. Average yield = 97.4%

IO-824: Received none from vendor this month. All have been tested.

Total: 3078 have been completed and ready for shipment. Average yield 98.8%

IO-823: Received 1728 from vendor since last report. 1056 are being tested.

Total: 7043 have been completed and ready for shipment. Average yield 99.4%

1.3.6 System Integration

1.3.6.1 Pedestal

1.3.6.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Start Barrel Pedestal Delivery to CERN	31-Dec-01	31-Dec-01	1-Mar-02	Delayed (See #1)
Start EC Pedestal Delivery to CERN	31-Dec-01	31-Dec-01	1-Mar-02	Delayed (See #2)
Start Ped.s deliveries Ship In Place	31-Dec-01	--	31-Dec-01	On Schedule
25% Pedestals Delivery from Vendor Compl	30-Jan-02	--	30-Jan-02	On Schedule
25% Bar & EC Ped.'s Deliveries to CERN Compl	29-Mar-02	--	29-Mar-02	On Schedule
50% Pedestals Delivery from Vendor Compl	29-Mar-02	--	29-Mar-02	On Schedule

Note #1-2 Delay matches installation schedule

Helio Takai (Brookhaven National Lab.)

We have received the prototype pedestal for the HEC cryostat. Mechanically it meets the requirements.

1.3.6.2 Cables/Base Plane

1.3.6.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
1st Delivery Date to CERN	31-Dec-01	--	30-Mar-02	Delayed (See #1)
1st Delivery Ship in Place	31-Dec-01	--	31-Dec-01	On Schedule

Note #1 Warm cables to be shipped with crate.

Helio Takai (Brookhaven National Lab.)

Baseplanes are in production.

1.3.6.3 Crate-Mechanical

1.3.6.3.3 Production

Milestone	Baseline	Previous	Forecast	Status
25% Crates Deliveries from Vendor Compl	30-Jan-02	--	30-Jan-02	On Schedule
25% Crates Delivered to CERN	29-Mar-02	--	29-Mar-02	On Schedule
50% Crates Deliveries from Vendor Compl	29-Mar-02	--	29-Mar-02	On Schedule

Helio Takai (Brookhaven National Lab.)

Prototype crate for the HEC has been received. The crate is similar to the one used in the Barrel system.

1.3.6.4 Power and Services

1.3.6.4.2 Prototype **Helio Takai (Brookhaven National Lab.)**

Prototype brick has been received and we have been testing for radiation resistance and magnetic field susceptibility. The power supply met the requirements for total ionizing dose and single event effects by a large margin. We are planning a test with neutrons and magnetic field. This should complete our qualification. In parallel we did a qualification for the most sensitive item, the power MOSFET. We have purchase a single batch of MOSFETs. Random tests with MOSFETs indicate good radiation properties. More importantly they are all similar as far as radiation is concerned.

Although low dose rate effects are important we have decided not to carry out the test because the power supply survives 10X the required values. Therefore there is enough safety margin for the power supplies even in the worst condition of low dose rates. We have decided against a single test, i.e. only proton irradiation, because we judge the test being valid ONLY for single event effects. The evaluation is based on consultation with experts from Vanderbilt University on radiation effects in semiconductors.

1.3.6.4.3 Production

Milestone	Baseline	Previous	Forecast	Status
25% Bus Bars Delivered from Vendor	30-Jan-02	--	30-Jan-02	On Schedule
50% Bus Bars Delivered from Vendor	29-Mar-02	--	29-Mar-02	On Schedule

1.3.6.5 Cooling

1.3.6.5.2 Prototype **Helio Takai (Brookhaven National Lab.)**

We are examining the possibility of having shorter cooling plates.

1.3.6.5.3 Production

Milestone	Baseline	Previous	Forecast	Status
Cooling Liquid Decision	17-Dec-01	--	17-Dec-01	On Schedule

1.3.7 Front End Board

1.3.7.1 FEB

1.3.7.1.1 Design **John Parsons (Columbia University)**

The design of the prototype ATLAS FEB was finalized, and the board submitted for PCB fabrication. Apart from the delayed rad-tol Vregs, all parts for the first board are in hand, so the PCB assembly will take place in November.

The FEB Critical Design Review was successfully held on Oct. 24 at Nevis.

During the October LAr week, the final choice (DSM vs. DMILL) for the SCA Controller was made, with DSM being selected. We will, therefore, also use the DSM version of the GainSelector, and the DSM CLKFO chip.

1.3.7.1.2 Pre-Proto/Mod 0/Atlas Prototype

Milestone	Baseline	Previous	Forecast	Status
Rad Tol. FEB Design Review	1-May-01	--	24-Oct-01	Completed
1st Delivery of Layer Sum Boards	2-Jul-01	--	1-Jan-02	Delayed (See #1)
Critical Design Review	3-Sep-01	--	24-Oct-01	Completed
Start Assembly	11-Sep-01	--	11-Nov-01	Delayed (See #2)
Rad Hard. - All Components	28-Sep-01	--	28-Feb-02	Delayed (See #3)
Final Dec. DMILL/IBM	7-Dec-01	7-Dec-01	15-Oct-01	Completed

Note #1 Delayed until boards are needed for rad-tol FEB production.

Note #2 Delayed due to the delay in the Critical Design Review.

Note #3 Delayed due to late delivery of rad-tol voltage regulators.

1.3.7.1.5 Radiation Testing **John Parsons (Columbia University)**

Our next run at Harvard will be Nov. 17/18. It is planned to irradiate some additional samples of FEB components, as well as the new Taiwanese optical transmitter.

1.3.7.2 SCA

1.3.7.2.1 Design — John Parsons (Columbia University)

The ATMEL PRR was held on Oct. 9 at CERN, and a target yield of 65% was agreed. The final ATLAS PRR for the SCA has been scheduled for Nov. 12, again at CERN. It is planned to submit the production immediately after the PRR, and SCA delivery should then be complete by mid-2002.

We are making measurements of 16 DMILL chips we have mounted on a Module 0 FEB, as part of the preparations for the PRR.

1.3.7.4 Optical Links

1.3.7.4.1 Design — John Parsons (Columbia University)

The optical link group, led by SMU, is aiming for a PRR in Feb. 02. The next steps are delivery of the DMILL SingleMUX chip, delayed until Nov., and radiation tests at Harvard of the new version of the Taiwanese optical transmitter. The order to Agilent for the GLink transmitter and receiver chips has been submitted by SMU.

1.3.7.4.2 Prototype/Module 0

Milestone	Baseline	Previous	Forecast	Status
Optical Links ATLAS Prototype	1-Jun-01	--	1-Jun-02	Delayed (See #1)

Note #1 Prototype completed and tested. FEB-end integrated with the layout. ROD-end will depend on the ROD design.

1.3.8 Trigger Summation

1.3.8.1 Layer Sums

1.3.8.1.3 Production (Qty = 3,441 Boards)

Milestone	Baseline	Previous	Forecast	Status
Start Deliveries to FEB (ORSAY/Nevis)	2-Jul-01	--	1-Jan-02	Delayed (See #1)

Note #1 Delivery will be started to Nevis only when requested.

Bill Cleland (University of Pittsburgh)

During the month of October the tests of LSBs have continued. We have completed an additional 550 boards during this period, including the modified S1x16 boards with gain=2. All of the modules have been burned in, and the testing of all boards should be finished by the end of the year.

1.3.8.2 Interface to Level 1

1.3.8.2.1 Design/Electronic Tooling/Comp. Specs

Milestone	Baseline	Previous	Forecast	Status
Circuit Design of ATLAS receiver Complete	12-Aug-01	16-Nov-01	30-Jan-02	Delayed (See #1)
Final Design Complete	4-Oct-01	30-Jan-02	30-Mar-02	Delayed (See #2)
Critical Design Review	12-Dec-01	30-Mar-02	30-May-02	Delayed (See #3)

Note #1 The investigation of a lower noise solution to the variable gain amplifier in the receiver signal chain has led to a delay of about 6 months in the design of the system.

Note #2 It is likely that this milestone will be missed by a few months, due to the delay arising from the study of the variable gain amplifier mentioned above.

Note #3 This milestone has slipped, since the production of the prototype module is delayed.

1.3.8.2.2 Prototype **Bill Cleland (University of Pittsburgh)**

Prototype boards for each of the functions carried out in the receiver have been built, with the exception of the variable gain amplifer (VGA). The VGA board has been delayed due to the reexamination of the type of chip to be used for the amplifier. Tests on a high-speed multiplying DAC have gone well, and this appears to be a viable low-noise alternative to a voltage controlled amplifier. Tests of waveform fidelity, gain (voltage to DAC current conversion ratio), noise, and delay are currently being carried out and documented. Tests of the monitoring function can be made with the prototype boards already produced, and these will be carried out within the next few weeks.

1.3.8.2.3 Production (Qty - 187 Boards)

Milestone	Baseline	Previous	Forecast	Status
Production Readiness Review	4-Mar-02	4-Mar-02	4-Oct-02	Delayed (See #1)
Start Production	4-Mar-02	4-Mar-02	4-Nov-02	Delayed (See #2)
PM Appr of RCV/Mon Bds Purch Req.'s	18-Mar-02	18-Mar-02	18-Nov-02	Delayed (See #3)

Note #1 The Receiver system design has been delayed by about 1 year as discussed above. The design review should be held at the end of 01, and we anticipate holding the PRR in Oct of 02.

Note #2 We will start production once the bid has been selected.

Note #3 We anticipate approval of the PM to proceed with production shortly after the PRR.

1.3.9 ROD System

1.3.9.1 ROD Board

1.3.9.1.1 Design

Milestone	Baseline	Previous	Forecast	Status
Reconstruct E, T, and chi square for TB data	12-Feb-01	--	1-Nov-01	Delayed (See #1)
Complete Code to form averages of Cal.	18-Jun-01	--	1-Mar-02	Delayed (See #2)
Complete Code to get OFC from CAL. Data	4-Sep-01	--	1-Mar-02	Delayed (See #3)
Real time evaluation of optimal filter coeff.	3-Dec-01	--	1-Apr-02	Delayed (See #4)
Conceptual Design Review	15-Jan-02	--	1-Jun-02	Delayed (See #5)

Note #1 Done, not completely reviewed.

Note #2-4 Calibration procedure not completely defined.

Note #5 First 2 samples with errors were available end of October.

1.3.9.1.2 Prototype

Milestone	Baseline	Previous	Forecast	Status
Decision Taken on Processor Hardware	10-Dec-01	--	10-Jun-02	Delayed (See #1)

Note #1 New conceptual design separates processor hardware from motherboard. This allows for evaluation of new DSP

Rod Engelmann (SUNY Stony Brook)

In October the following work was done:

BNL/Stony Brook - ROD demo tests: the high trigger rate (<~ 100kHz) runs with the ROD equipped with one PU were continued. An error rate of 4 events out of ~$2x10^8$ events was observed running at 100kHz in 16k events bursts which filled the ROD output memory buffer. Work on a busy logic for 32 sample readout is in progress.

Nevis: LAP and Nevis prepared a PU (2 DSP's) architecture and presented it at the October LARG ROD technical meeting. A PU for the demonstrator ROD will be built. In the BESG October meeting the choice of DSP was moved to 2002. An 8 DSP ROD (4 dual DSP PUs) with data routable from any input to any PU position for staged installation seems to be the preferred ROD.

SMU: Two samples of the TI C64 DSP were obtained and sent to Nevis.

1.3.10 Forward Calorimeter

1.3.10.1 FCAL1 Module

1.3.10.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
FCAL1-C Interconnects Complete	30-Apr-01	30-Nov-01	30-Dec-01	Delayed (See #1)
FCAL1-C Tube Swaging Complete	1-Oct-01	--	30-Oct-01	Completed (See #2)
FCAL1-A Matrix Plate Inspection-1	10-Dec-01	--	10-Dec-01	On Schedule (See #3)
FCAL1-C Module Complete	15-Mar-02	--	15-Mar-02	On Schedule (See #4)
Delivery 2nd half - FCAL1-A	18-Mar-02	--	18-Mar-02	On Schedule (See #5)
FCAL1-A Matrix Plate Inspection-2	25-Mar-02	--	25-Mar-02	On Schedule (See #6)

Note #1 We decided to send out only half of the interconnect boards to have the sockets installed. This is to provide better QC and to encourage low pricing. This will delay completion a bit but not seriously.

Note #2 Completed a week early.

Note #3 Inspection has started and is progressing quickly. Seven plates have already been measured.

Note #4 We still hope to make this date.

Note #5 The second shipment arrived on 24 October but the two endplates will be delivered later due to change orders.

Note #6 This should start as soon as inspection of the first batch is completed, all but for the two end plates.

John Rutherfoord (University of Arizona)

FCal Construction:

In August we were asked by ATLAS management, following a point raised by the LHCC Comprehensive Review team, to investigate what it would take to advance the FCal production schedule by about three months so that our calibration test beam run could start in early June of 2003 rather than in late August 2003. We presented this study in writing at end of August and made the point that any speed-up would have to be decided quickly because we can't recover lost time too late in the game. We made a detailed analysis which showed that a decision would have to be reached by end of September in order to achieve a full three months speed-up. A decision after this time would yield less than a three-month speed-up. We did not receive a response to our analysis by end of September and quickly found out why. The announcement of large cost over-runs in the LHC project raised many questions about future strategies, of which the FCal is just one small part. So a decision was put off indefinitely. Nevertheless we featured the FCal production schedule in the FCal ASSO in early October. While the ASSO was meant to cover all

aspects of the FCal system we concentrated on the problem areas to good effect. We were pleased that the ATLAS management paid close attention to the issues we raised.

It was announced that the delivery of the EndCap C cryostat is delayed by about 1.5 months due to a leak in the Omega seal in the cold bulkhead during the pressure test at SIMIC. The delivery date is now 3 December. This could delay the availability of the support tube which we need early in the final assembly process which is presently scheduled to start at CERN next summer.

Leif Shaver is planning a trip to Canada for 7-9 November. He is also looking into a trip to SIMIC with Mircea Cadabeschi to inspect the EndCap A cryostat support tube to make sure the inner dimensions will accept the FCal modules and the Plug3. There have been delays in ordering the plugs 1, 2, and 3 from the winning bidder in Australia. There seem to be communication problems between CERN and our Australian colleagues who are providing these plugs as a common projects contribution. We are trying to expedite this order but are not in a good position to do a lot.

The original plans for the FCal Calibration Test Beam run assumed that some of the electronics experts would be available to setup and run the warm electronics as was the case in the early barrel and EMEC test beam runs. As a small group it is not practical for the FCal community to provide the level of expertise required to manage this complex system. However because of pressures to build the electronics it appears that such experts will not be available for any more than some advice and assistance in procuring the parts. We suspect this will not be enough to ensure the success of our calibration run.

Periodically we update our FCal construction schedule so that our key milestones are in line with the changing LArG and ATLAS schedules. Thus the schedule we refer to in these reports is not the schedule that the Project Office keeps. Over the last year our FCal construction schedule has been more aggressive than the Project Office schedule because the LArG has tried to advance its schedule and we've complied. Also there was some mistake in the Project Office schedule.

FCal1 Module:

The latest version of the swage tool held together long enough to finish swaging all the tubes in the FCal1C module. We have finished this task about two months behind our production schedule. We still have a few things to do before we move on to the next step, inserting the electrode rods. These small tasks are 1) swaging the tubes around the tie rods which are obscured by the tie rod bolt head (2 days), 2) re-swaging some `loose' tubes (2-3 days), and 3) removal of about 30 tubes sticking out of the module after swaging and replacing them. They are supposed to be flush or slightly recessed from the outer face of the end plates. Before this last task we plan to practice on some tubes from Module 0.

The last five copper absorber plates for the FCal1A matrix arrived from the STC machine shop at Carleton last week (two days ahead of the contract delivery date). The two end plates are delayed because of the changes we requested due to the FCal symmetry change and because some of the plates were not sufficiently flat. These are not on the critical path.

We hired a second engineering aide who started Friday. He was a tech at Fermilab for many years working mostly on CDF. (The engineering aide we hired in July worked at BNL in cryogenics.) His first assignment is to acceptance test and characterize the FCal1A absorber plates. We are also trying to hire a third (half-time) engineering aide (with no HEP lab background) to help with the cold electronics which is falling behind schedule too. This additional manpower should help us get back on schedule. The

engineering aide we hired in July was always a part of our plan but the former Fermilab person and the potential half-time person are not.

About 13,417 copper electrode rods have passed the pinhole gauge out of the 19,864 checked so far. There are about 6,000 rods left to be checked. We require 12,260 for FCal1C so we have enough to proceed with this module. About 6,500 of these rods are ready for insertion. The rest still need to be inspected for cleanliness. The pin-gauge failures will be re-drilled from the other end and then re-cleaned. We are worried that we won't have enough for FCal1A and may have to order some more.

The signal pin and ground pin insertion tools are back from the shop. The PEEK fiber feeder (with a cleaner stage) is ready to go. We plan to test these this week so that rod insertion can start up smoothly in about two weeks.

While we are behind our construction schedule for the C end, we can still easily meet the date for delivery of the FCal1C module to CERN in time to start the final assembly. The present schedule has quite a few months of float between completion of this module and delivery. The reason is that we intend to start the FCal1A module before part of our team moves to CERN next summer. It is this plan which suffers as we fall behind. We are hoping that we have been very conservative in the schedule for rod insertion and that we can make up time during this phase. We will know shortly when we get some experience with rod insertion.

1.3.10.2 FCAL Electronics

1.3.10.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
PCBs received at AZ	21-Nov-00	15-Dec-01	31-Jan-02	Delayed (See #1)

Note #1 Revision A of the board is stuffed and is being tested. There will be a Revision B to correct a few flaws. The board production should be completed soon thereafter.

John Rutherfoord (University of Arizona)

Cold Electronics:

The fabrication house which is making the transmission line transformers ran into a small problem with the carrier height off the summing boards. The peek fiber which holds the ferrite core to the carrier also holds the carrier off the summing board making it harder to solder the connectors to the summing board. They have suggested a fix which involves grooving the carrier and have produced 100 assemblies for us to test. These are in the mail now.

The cable testing facility is nearly ready to go. Final run-through is in progress and we expect the first cooldown quite soon. The plan is to complete one cooldown per week. In each cooldown we plan to test 10 cable harnesses, each with 64 cables. With a total of 240 cable harnesses we project at least 24 weeks of testing.

While we are well behind our schedule on this too, we put this early in the schedule so that we would not be leaving many things until the end. We want time at the end to take care of emergencies and other

unforeseen tasks. So we will continue to push to get this back on our original schedule, despite the apparent lack of urgency.

1.4 TILE

Milestones with changed forecast dates:

1.4.4.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Scintillator procurement	1-Oct-00	1-Nov-01	1-Dec-01	Delayed (See #1)
Start Scintillator Assembly	1-Dec-00	1-Dec-01	1-Feb-02	Delayed (See #2)

Note #1-2 We are making final modifications to the scintillator design. Procurement will follow as soon as final drawings are approved, and funding to buy extension scintillators IS available at MSU.

1.4.4.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
Management Contingency Go-Ahead	1-Oct-01	1-Oct-01	1-Oct-02	Delayed (See #1)

Note #1 Status unknown.

1.4.1 Extended Barrel Mechanics — James Proudfoot (Argonne National Lab.)

Good progress was made in all areas of mechanics in October.

184 submodules have been completed at the University of Illinois and shipped to Argonne (a total of 189 are stacked at this location). The total of completed submodule at Argonne now stands at 189. In addition, excellent progress has been made on repairing the submodules from the University of Chicago with only one of these remaining to be repaired. The decision on how to proceed with the remaining submodules from the University of Chicago which have deformed slots will be made in November. It is likely that some of these will be useable, with care during instrumentation. All sites are expected to complete their complement of 192 submodules in November.

44 modules have been completed and work on Module 45 is far along. A problem was detected with the endplate alignment on Module 40 during instrumentation and was similar to a problem detected during QC on Module 44. Corrective measures are being evaluated and in the meantime we are re-checking all modules which are still in the US. We anticipate that the simplest corrective procedure will be successful and this will be carried out on Module 40 in early November.

Module testing is also proceeding well and presently a total of 36 modules have been tested and shipped to CERN. We expect to make at least one more shipment before the end of 2001.

Excellent progress has also been made in engineering work. The design for the extended barrel saddles is essentially final. The design of the special cut submodules is complete and undergoing TileCal engineering review for production approval. The preparations at Argonne to do this work are almost complete, with drawing packages prepared and details worked through with Argonne Central Shops who will perform this work.

1.4.1.1 Submodules
1.4.1.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Submodule Completion (509 Cum)	14-Dec-01	--	14-Dec-01	On Schedule
Submodule Completion (576 Cum)	15-Mar-02	--	15-Mar-02	On Schedule
Submodule Construction Complete	15-Mar-02	--	15-Mar-02	On Schedule

Victor Guarino (Argonne National Lab.)

During the month of October nine submodules were constructed at ANL. In addition, three UC submodules were disassembled and repaired. No problems were encountered during production and regular maintenance on the production equipment was performed. The drive belts on the Timesaver machine broke early in the month and had to be replaced.

Steven Errede (University Illinois-Urbana-Champaign)

In October 2001 we made 8 ATLAS TileCal submodules. We have now made a total of 190 submodules (only 2 more to go!) We shipped 16 fully completed submodules to ANL in mid-October, thus a total of 184 submodules have now been shipped to ANL.

We will complete ATLAS TileCal submodule production at UIUC in the first week of November. We intend to ship the final 8 ATLAS TileCal submodules and remaining spare parts - e.g., master & spacer plates, spring pins, paint, etc. to ANL in ~ mid-November.

1.4.1.2 Extended Barrel Module
1.4.1.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
Last Delivery of Girders	21-Dec-01	--	21-Dec-01	On Schedule
Module Completion (50 Cum)	31-Jan-02	--	31-Jan-02	On Schedule
Modules Shipped to CERN (40 Cum)	31-Jan-02	--	31-Jan-02	On Schedule

Victor Guarino (Argonne National Lab.)

During the month of October three modules were constructed, ANL43, 44 and 45. No problems were encountered during production.

The first special modules will be constructed beginning with module #48. The first special modules will be special only because they have submodules with 5-hole weld bars. Starting with module #56 the special modules will have cut submodules in them. Construction prints to help the machine shop layout and cut these submodules were constructed during the month. In addition, several assembly prints were made to help keep track of the location of the special submodules in each special module and in the EB.

Work also continued on the structural analysis of the EB. The analysis of the EB when subjected to magnetic, seismic, and gravity loading was completed. It was found that under this extreme loading condition that the support saddles have stresses and deflections in acceptable limits. The analysis of the back cryostat support, however, under similar loading conditions found that the stresses and deflections in

the bolts attaching it to the saddles were unacceptably high. In order to remedy this situation several additional analysis were carried out during the month to examine additional ways of supporting the Z direction seismic loading on the back cryostat support. Various ways of transferring this load to the EB by rods through the source tubes holes were investigated. In addition, a third stiffener was added to the back cryostat support. It appears at this time that will be possible to approach a seismic load of .15g on the back cryostat support plate using these additional methods.

A complete 3D solid model of the EB saddles was also started at the end of October. This model will be used for integration purposes, to test for clearances of the tools needed for assembling the EB, and to create a very detailed FE model of the saddles. This model can be seen at http://gate.hep.anl.gov/vjg/ in files EB1.tif and EB2.tif.

1.4.1.4 Testing

Milestone	Baseline	Previous	Forecast	Status
Beam test Series A	2-Oct-01	--	2-Oct-01	Completed
Modules Source Tested (40 Cum)	31-Dec-01	--	31-Dec-01	On Schedule

1.4.2 Extended Barrel Optics
1.4.2.1 Extended Barrel Scintillator
1.4.2.1.1 Design

Robert Miller (Michigan State University)

Optical Instrumentation Summary
Instrumentation of the US Tilecal extended barrel modules continued on schedule in October. One module was completed at MSU and one was completed at ANL. A total of 39 modules have been instrumented, 38 have been tested, and 4 additional modules are in various stages of production.

1.4.2.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
100% Tile Deliveries from Russia Compl	2-Jul-01	--	2-Dec-01	Delayed (See #1)

Note #1 Tiles are at CERN and have been sorted for distribution to the 4 instrumentation sites. The final shipment is expected next month, November. Some exchange of tiles from ANL to MSU will be done to keep the instrumentation on schedule.

David G. Underwood (Argonne National Lab.)

Module ANL-40 was finished during October except for the final tie-down. We started choosing tile packs for module 42. Module 40 had the lowest rms variation from the CS source scan of any US module so far. This was 3% with the Nodulman method, and 5% with the ANL version of the CERN method of analysis.

Robert Miller (Michigan State University)

Module 38 was scanned with the LED source at MSU and shipped to ANL in exchange for Module 43. Module 38 has several bad fibers in one cell that could not be repaired by our usual techniques. After some discussion with collaborators, we have agreed to attempt some further repair work on this module at

ANL. Module 43 was prepared for instrumentation, and had tiles inserted. Module ANL-39 was completed at MSU after fixing a broken blade and relapping the diamond on the polishing machine. Fibers were inserted and routed in Module 41.

The final batch of tiles have been shipped from CERN and is expected to be distributed to MSU in November.

1.4.2.2 Extended Barrel Fibers
1.4.2.2.3 Production **David G. Underwood (Argonne National Lab.)**

Module ANL 36 was completed, and Fibers were installed in module ANL-40. There was only 1 repair and Module 40 had the lowest rms variation measured with the Cs source scan of any US module so far.

We are still removing potentially defective fibers before the gluing operation. They are found by two different scans, one with the camera inside the girder using room light outside to excite the fibers, and one using a blue LED flashlight and visual inspection.

1.4.2.4 Supplies
1.4.2.4.3 Production **David G. Underwood (Argonne National Lab.)**

We received two boxes of profiles from Lisbon. We sent one directly to MSU, and are holding off on unpacking the second because it is difficult to split full boxes, and MSU may need more if their production rate continues.

1.4.3 Readout
1.4.3.1 PMT Block
1.4.3.1.3 Production **Steven Errede (University Illinois-Urbana-Champaign)**

We have spent the month of October working on getting the Step2 ATLAS Tilecal PMT testing hardware and software operational. We are making good progress, but we have a ways to go before we can commence with Step2 PMT testing. We hope this activity will be completed in November. We will begin Step2 testing of PMTs as soon as we are ready.

1.4.3.2 Front-end 3-in-1 Card
1.4.3.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
3-In-1 Card Test 100% Complete	30-Nov-01	--	30-Nov-01	On Schedule (See #1)
3-In-1 Card Final delivery to CERN	1-Mar-02	--	1-Mar-02	On Schedule

Note #1 Routine testing should be complete by 30-Nov-01 but residual repair work may extend several additional months.

James Pilcher (University of Chicago)

As noted previous months all 3-in-1 cards have been produced and delivered to Chicago. Burn-in and testing are in progress. In October 1123 cards passed these steps and were shipped to CERN. This brings the total shipped to 8,900 or 84% of the required total.

To date, faulty or questionable cards have been put aside. In November we will have to begin working on these cards. As a result, the throughput is expected to decrease.

1.4.3.3 Front-end Motherboards
1.4.3.3.3 Production

Milestone	Baseline	Previous	Forecast	Status
MB Card Test 10% Complete	1-Mar-01	--	31-Oct-01	Completed
MB Card Test 25% Complete	1-May-01	--	1-Dec-01	Delayed (See #1)
MB Card Test 50% Complete	1-Aug-01	--	1-Jul-02	Delayed (See #2)
MB Card Test 100% Complete	24-Dec-01	--	24-Dec-02	Delayed (See #3)
Final Delivery to CERN	1-Mar-02	--	1-Mar-03	Delayed (See #4)

Note #1-4 Motherboard testing started late because of vendor delays (slow fabrication of bare PCBs and an extra pre-production cycle to confirm specifications). This task is now proceeding at the planned rate but completion is delayed. Completion in Dec/02 still provides over 1.5 years float in the ATLAS schedule.

James Pilcher (University of Chicago)

All 4 sections of the Motherboard system, together with the mezzanine board used for control purposes, have been produced and received at Chicago. Work continues to burn-in and test the boards.

In October, 17 Motherboard sets were processed and shipped to CERN. This brings the fraction shipped to 12% of the required total. This work proceeds on a routine basis. The monthly throughput is expected to rise.

1.4.4 Intermediate Tile Calorimeter
1.4.4.1 Gap Submodules
1.4.4.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Scintillator procurement	1-Oct-00	1-Nov-01	1-Dec-01	Delayed (See #1)
Start Scintillator Assembly	1-Dec-00	1-Dec-01	1-Feb-02	Delayed (See #2)
Ship submodules 45-48 to ANL	26-Nov-01	--	26-Nov-01	On Schedule
Ship submodules 45-48 to BCN	17-Dec-01	--	17-Dec-01	On Schedule
Ship submodules 49-52 to ANL	11-Feb-02	--	11-Feb-02	On Schedule
Ship submodules 49-52 to BCN	4-Mar-02	--	4-Mar-02	On Schedule

Note #1-2 We are making final modifications to the scintillator design. Procurement will follow as soon as final drawings are approved, and funding to buy extension scintillators is available at MSU.

Kaushik De (University of Texas at Arlington)

Two ITC submodules each were shipped to Argonne and Barcelona as scheduled. Production is continuing smoothly on schedule.

The new stacking tools are working very well for the special submodules. We are not experiencing any more perpendicularity problems. Our glue machine died for a few days and was fixed after consultation with the manufacturer. There should be no impact on production schedule.

We received the third set of 250 PMTs and started testing them. We found a problem with the dark current measurements and found that the Step 2 hardware had to be disconnected. This hardware was installed after batch two testing. After completion of Step 1 testing of this batch, we will resume setting up for Step 2. Currently, we have 750 PMTs at UTA waiting for Step 2 testing. The final software for Step 2 testing has not been released yet.

1.4.4.2 Cryostat Scintillators
1.4.4.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
Scintillator procurement	1-Dec-00	--	1-Dec-01	Delayed (See #1)
Start Scintillator Assembly	7-Sep-01	--	1-Feb-02	Delayed (See #2)
Management Contingency Go-Ahead	1-Oct-01	1-Oct-01	1-Oct-02	Delayed (See #3)
Complete CR testing	1-Feb-02	--	1-Dec-02	Delayed (See #4)

Note #1 Scintillator purchase and production of the ITC crack scintillators is delayed pending the decision to authorize this part of the project that was included in the management contingency fund. That decision is scheduled for 1 Oct. 01.

Note #2 Purchase of the mechanical components for the crack scintillators is awaiting final checks by the ATLAS technical coordination team.

Note #3 Status unknown.

Note #4 Fabrication start is delayed.

Robert Miller (Michigan State University)

Production of the ITC fiber assemblies continued during October. The final set of assemblies for the special type 9 modules was shipped to Barcelona in October. The next set of assemblies will be sent to ANL in November.

A set of AutoCAD drawings of the ITC scintillators will be made and submitted to the CERN drawing collection for approval. Assembly of these parts is still scheduled to begin early next year.

1.5 MUON

Milestones with changed forecast dates:

1.5.9.1.1 MDT-ASD

Milestone	Baseline	Previous	Forecast	Status
ASD PRR	19-Oct-01	19-Dec-01	31-Jan-02	Delayed (See #1)

Note #1 The ASD prototypes have undergone successful bench testing. The only issue was that the maximum programmable dead time is no larger than the maximum drift time. It is now important to do simulated production testing on a larger number of the chips and to test them out on a chamber with an octal mezz board prototype. The first tests of the octal ASD mounted on a Mezz board are now underway and should be completed by the end of the year.

1.5.9.1.2 Mezz PCB

Milestone	Baseline	Previous	Forecast	Status
Mezz PCB Certified	16-Nov-01	16-Dec-01	31-Jan-02	Delayed (See #1)

Note #1 The first octal mezz prototypes are currently being tested (4x6 boards). The plan is to test these as well as a 3x8 version extensively by the end of the year.

1.5.12.3.2 Proximity Monitors

Milestone	Baseline	Previous	Forecast	Status
Prox. Production 10% Complete	1-Jan-02	1-Jan-02	1-Jul-02	Delayed (See #1)

Note #1 For final design of the proximity monitors, we must know the position of all components to within 10 mm. Since the layout of ATLAS is not yet final, we are holding the start of production until the layout is final. Production can be completed quickly so this will have no overall schedule impact.

1.5.12.3.3 Multi-Point System (BCAM)

Milestone	Baseline	Previous	Forecast	Status
BCAM Production Begins	1-Jan-02	1-Jan-02	1-Jul-02	Delayed (See #1)

Note #1 Final BCAM production will not begin until after the PRR. This has not yet been scheduled.

1.5.12.4.18 EMS3 (Seattle)

Milestone	Baseline	Previous	Forecast	Status
Ship to Site	7-Sep-01	1-Apr-02	1-Jan-02	Delayed (See #1)

Note #1 This chamber is not scheduled to be built until the third round of MDT production. Since this is a special chamber, confirmation of the inplane design will await completion of the design of the chamber.

1.5.4 CSC Chambers

1.5.4.4 CSC Construction

Milestone	Baseline	Previous	Forecast	Status
Start CSC Chamber Production	1-Mar-01	--	1-Oct-01	Completed (See #1)

Note #1 Production of the first four chambers has now started.

Venetios Polychronakos (BNL)

The production has now started. We have in hand all materials for the first four chambers. We plan to carefully measure and fine tune each assembly step while the procurement process for the materials for the remaining chambers are being procured. The bid package for the cathodes (the longest lead time item) is out and the remaining orders are being prepared. We expect to be in full production mode within six months. At that point we estimate producing one chamber every working week.

In the final panel assembly procedure, we obtain all the components machined with both the alignment and mounting holes predrilled. We do the panel assembly at the production facility. No further finishing work of the panels is required.

1.5.4.4.1 CSC1

Milestone	Baseline	Previous	Forecast	Status
4 Chambers Complete	1-May-01	--	1-Dec-01	Delayed (See #1)
16 Chambers Complete	2-Oct-01	--	30-Apr-02	Delayed (See #2)

Note #1-2 This milestone follows the delay in start of construction, which has now started (October 1).

1.5.4.5 CSC Support Structure

Milestone	Baseline	Previous	Forecast	Status
Start Support Structures Construction	3-Jan-01	--	3-Dec-01	Delayed (See #1)

Note #1 The small wheel fabrication is expected to be launched by the end of the year. The contract and follow-up will be CERN responsibility.

1.5.7 MDT Chamber Production

1.5.7.1 Engineering Management

1.5.7.1.1 Chamber Integration Drawings

Milestone	Baseline	Previous	Forecast	Status
Complete Chamber Integration Drawings	1-Jul-01	--	1-Jun-02	Delayed (See #1)

Note #1 The next series of chamber integration drawings are for the third series of chambers EIS2, EML3 and EMS3. During October the EIS2 drawings were completed and we have stated the EML3 drawings.

Richard Coco (MIT)

The chamber integration drawing for the second series of MDT chambers EIS1, EMS4 and EMS2 were completed during the last reporting period. These are the Multi-layer and full chamber assembly drawings.

Further all drawings for the first six chamber types (EIL1, EMS5, EML2, EIS1, EMS4 and EMS2 have been posted to the CERN CDD drawing web site where they are now available to the US Atlas community and can be downloaded as required.

1.5.7.1.2 Engineering Documentation — Richard Coco (MIT)

Engineering documentation efforts are focused on multi-layer and chamber assembly drawings as well as the Faraday cage and gas system assembly drawings. Work on the drawings for the third series of chamber EIS2 have been initiated to be followed by drawings for the EML3 and EMS3. Design of the next shipping crate for the EIS2 chambers will be initiated during this reporting period.

1.5.7.1.4 QA/QC Engineering Support — Richard Coco (MIT)

QA/QC support to MDT chamber assembly and services installation is provided on an as requested basis.

1.5.7.1.5 Project Engineering — Richard Coco (MIT)

Project engineering activities include supervision of chamber drawing and documentation efforts as well as working with the Project Manager monitoring budgets, chamber construction schedules, gas bar machining schedules and other parts procurement activities. All common item procurement activities are based at Harvard and supervised by the project engineering office.

1.5.7.2 Design of Chambers and Tooling

1.5.7.2.1 Faraday Cages

Milestone	Baseline	Previous	Forecast	Status
Finished Faraday Cage Designs	21-Dec-00	--	22-Nov-01	Delayed (See #1)

Note #1 Focus on FC design is now on the HV power feed-in box and the mezz card shield boxes.

Richard Coco (MIT)

The remaining Faraday cage design activities include the HV power supply input box to each chamber and the Mezz card shielding box. The efforts continue in process paced somewhat by the continuing evolution of the electronics printed wiring board design.

Procurement of Faraday cage parts required for chamber assembly continues using the qualified vendor - Bay State Metals.

1.5.7.2.2 Gas System

Milestone	Baseline	Previous	Forecast	Status
Finish Gas System Design	7-Jun-01	--	28-Sep-01	Completed
Gas System	15-Aug-01	--	28-Sep-01	Completed
Gas System	28-Sep-01	--	28-Sep-01	Completed
Gas system	22-Nov-01	[New]	15-Feb-02	Delayed (See #1)
Gas system	22-Nov-01	[New]	15-Feb-02	Delayed (See #2)

Note #1 Gas system final design has been delayed due to the need to find a qualified vendor for the large tubing which carries gas to the manifold gas bars.

Note #2 Delay in completing the gas system design is the result of seeking a qualified vendor for the large gas feed tube which distributes gas to the manifold bars.

Richard Coco (MIT)

Gas system design has largely been completed and procurement is in process for gas manifold bars, feed tubing and capillary tubes. During the last reporting period an order for 6-mm OD, 5-mm ID brass gas tubing, which distributes gas from the chamber Noryl inlet block to each multi-layer gas manifold, was issued to H&H Tubing. Delivery is scheduled for mid-November.

1.5.7.2.3 Spacer Frame Design

Milestone	Baseline	Previous	Forecast	Status
Finish Spacer Frame Design	17-Jan-02	--	17-Jan-02	On Schedule

1.5.7.2.4 Chamber Analysis

Milestone	Baseline	Previous	Forecast	Status
Finish FEA Modeling	30-Aug-01	--	30-Nov-01	Delayed (See #1)

Note #1 This work has been delayed because the final wheel structural designs are not yet available. ISTC team to come to CERN in Nov. 01 to complete design.

The design review of the Big Wheel (BW) took place Nov. 20, 2001 and was successful - with the caveat of several matters of interference to be cleared up. The FEA presented should provide the needed information to complete the integration of chamber mounts with the BW (remarks by F.E. Taylor).

1.5.7.2.5 Design of Special Chamber Tooling

Milestone	Baseline	Previous	Forecast	Status
Finish all Special Chamber Tooling	27-Sep-01	--	28-Dec-01	Delayed (See #1)

Note #1 Completion of this task will probably be delayed but will be ahead of need. Work is concentrated at Brandeis on EMS3 - the first special chamber that will be constructed.

1.5.7.3 Tooling

1.5.7.3.1 Module 0-Precision Tooling

1.5.7.3.3 Series Production Precision Tooling

Milestone	Baseline	Previous	Forecast	Status
Finish Series Production Tooling	1-Feb-01	--	15-Jan-02	Delayed (See #1)

Note #1 Design work for the series 3 production is underway. The tooling design remains off the critical path.

1.5.7.3.5 BMC Tube Assembly Station — Krzysztof Sliwa (Tufts University)

Machining of 48 of threaded aluminum leak-test caps was completed during the month. The production set was delivered to the BMC tube factory at Harvard during last week of October. Preparations were underway at end of the month to transport the sphere blocks and trophy pieces machined at Tufts to the Harvard shop for finishing.

Frank Taylor (MIT)

The BMC assembly station continues to operate. Some alignment work was performed on the swagger coils. To date 4141 EIS1 tubes have been assembled.

1.5.7.3.8 BMC Tube Test Station — Frank Taylor (MIT)

The QA wire tension and dark current tester was accidentally damaged last month. HV was accidentally introduced into the readout electronics front end. The device is now fixed by Brandeis and a safety circuit implemented.

1.5.7.3.11 BMC Chamber Assembly Station — Alex Marin (Boston University)

We received from Brandeis the drawings needed for EIS1_C chambers. The parts are manufactured at HEPL.

1.5.7.6 Common Procurement

1.5.7.6.1 Procurement of Tubes — Tom Fries (Harvard University)

Fabrication of the 4th series has begun consisting of:

Batch #80 BMC (EIL2)

Batch #76 BMC (EIL3)

Batch #82 UW (EIL4)

Batch #83 UM (EML4)

1.5.7.6.2 Procurement of Wire — Tom Fries (Harvard University)

No additional wire was received in October.

1.5.7.6.3 Procurement of Endplugs — Tom Fries (Harvard University)

4,600 NIEF Endplugs were received and distributed among the US assembly sites.

1.5.7.6.4 Procurement of Faraday Cage — Tom Fries (Harvard University)

No additional Faraday Cage parts were received in October.

1.5.7.6.5 Procurement of Gas Supply System — Tom Fries (Harvard University)

Tubelettes:

The European supplier (Heim) has delivered 35% of their order. This order accounts for roughly 70% of our total tubelette requirements.

Gas Bars (from UW machine shop):

EMS-4 Type III - 32 bars (8 chamber's-worth) delivered to UM.

EIS-1 Type III - 32 bars (8 chamber's-worth) delivered to BMC.

1.5.7.7 BMC Chamber Construction 104

1.5.7.7.2 EIS1 series (WBS 1.5.7.7.2) — Alex Marin (Boston University)

As of 10/31 we predict the completion of Mod 24 (last of EIS1_A series) on Nov 2nd, including all the retooling for the C type chambers, as well as all most of the calibration and BCAL measurements.

Frank Taylor (MIT)

To date 4141 EIS1 tubes have been made. A third technician is now on board who has greatly increased the production assembly of endplugs.

1.5.7.8 WBS 1.5.7.8 Michigan Chamber Construction 104

1.5.7.8.2 EMS4 Series (WBS 1.5.7.8.2) **Ed Diehl (University of Michigan)**

We continued building series 2 chambers (EMS4) completing a total of 10.5 series 2 chambers by the end of the month. Faraday cage & gas manifold installation & chamber gas certification now are done concurrently with chamber production. After chamber gluing is completed, the chamber is moved to a rolling table outside the glue room where the services work is done. We have had no further problems with pinhole leaks.

We temporarily ran out of NIEF endplugs and switched to the backup MPI plugs. However, we immediately found that the MPI plugs we not acceptable as several tubes made with them suffered from leaking, possibly due to porous Noryl.

We remeasured the comb alignment with the BCAL and wire microscope at the midpoint of EMS4 production. We found that the angle combs had moved about 10 microns out of alignment, possibly because the H-blocks had not been used to secure the angle combs. The straight combs, which did use H-blocks did not walk. We re-aligned with combs with shims and snugged up the H-blocks to discourage further walking. We also re-checked angle comb flatness and found that the combs were still flat.

A chamber can be done in 7 days, whereas tube stringing takes 8 days. In November, chamber gluing should catch up to tube production at which point chamber production will drop back to 8 days/chamber.

We began planning for the EML3 retooling which should take place in January 2002. We began gathering drawings and starting machining. We are designing a new chamber cart to handle the large EML chambers.

1.5.7.9 WBS 1.5.7.9 Seattle Chamber Construction 96

1.5.7.9.2 EES2 series* (WBS 1.5.7.9.2) **Henry Lubatti (University of Washington)**

It was necessary to stop production of drift tubes for two days because we had no end plugs.

We attempted to use some of the MPI end plugs but found that the aluminum on most was so badly oxidized and concluded that this might compromise the ground connection; in addition they were full of chips and proved very difficult and time consuming to clean.

Despite these "road-blocks" we completed 938 EES2 drift tubes in October.

1.5.8 MDT Supports

1.5.8.1 Mechanical Design

1.5.8.1.3 Integ with Support Structure

Milestone	Baseline	Previous	Forecast	Status
(SM Wheel) CERN Design/FEA Complete	15-Jul-00	--	1-Dec-01	Delayed (See #1)
(Big Wheel) CERN Design/FEA Complete	1-Feb-01	--	15-Dec-01	Delayed (See #2)
50% Complete	1-Aug-01	--	1-Nov-01	Delayed (See #3)

Note #1 A large fraction of this work has been completed, but as we depend on CERN for the detailed small wheel design from CERN and others for alignment bar and plumbing information we have a delay. Some small progress was made in July. We forecast that this will not be completed until December 1, 2001. (Situation unchanged since July 01 report.) Status unchanged since last month. BW design review took place Nov. 21, 2001 which should help to clear this bottleneck.

Note #2 Because we depend on CERN for the detailed big wheel design and others for alignment bar and plumbing information we have a delay. We forecast that this will not be completed until March 15,2002. The May design report on the Big Wheel showed much progress but the final drawings and bid specs will not likely be available until Dec, 15, 2001. It is expected that there will be further design and installation changes during the bid process. (Status unchanged since July 01 report.)

Note #3 Delayed for same reasons as noted above.

Henry Lubatti (University of Washington)

Colin Daly attended the October ATLAS week to interface with the engineers designing the big wheel and presented his FEA of the small wheel. Colin obtained a copy of the Big Wheel FEA done by our Russian colleagues for checking.

1.5.9 MDT Electronics

1.5.9.1 Mezzanine Card

1.5.9.1.1 MDT-ASD

Milestone	Baseline	Previous	Forecast	Status
ASD PRR	19-Oct-01	19-Dec-01	31-Jan-02	Delayed (See #1)

Note #1 The ASD prototypes have undergone successful bench testing. The only issue was that the maximum programmable dead time is no larger than the maximum drift time. It is now important to do simulated production testing on a larger number of the chips and to test them out on a chamber with an octal mezz board prototype. The first tests of the octal ASD mounted on a Mezz board are now underway and should be completed by the end of the year.

1.5.9.1.2 Mezz PCB

Milestone	Baseline	Previous	Forecast	Status
Mezz PCB Certified	16-Nov-01	16-Dec-01	31-Jan-02	Delayed (See #1)

Note #1 The first octal mezz prototypes are currently being tested (4x6 boards). The plan is to test these as well as a 3x8 version extensively by the end of the year.

1.5.9.1.3 Mezzanine card/MDT-ASD Test Start George Brandenburg (Harvard University)

The production ASD test stand is being developed and should be ready early next year. The development of the production Mezz test stand will follow.

1.5.9.2 Hedgehog Cards

1.5.9.2.1 Signal Hedgehog 3X8

Milestone	Baseline	Previous	Forecast	Status
Hedgehog PCB Certified	30-Aug-00	--	1-Nov-01	Delayed (See #1)
Hedgehog Production Complete	28-Feb-01	--	31-Dec-02	Delayed (See #2)

Note #1 Delayed to implement design changes: shortening, coating change, and capacitor vendor switch (Tucsonix to Murata). Final prototype testing is almost complete.

Note #2 Production will most likely now take place at CERN starting in the last quarter of 2001. The first production quantities should be available early in 2002. Production will continue during 2002 in parallel with chamber building.

1.5.9.2.3 Hedgehog Card Test Stand George Brandenburg (Harvard University)

This is being developed in conjunction with the Rome INFN group.

1.5.9.3 CSM-MEZZ cables

1.5.9.3.1 CSM-MEZZ cables George Brandenburg (Harvard University)

The first prototype CSM-Mezz cable has been successfully tested with the first octal Mezz prototype. Tests of various cable lengths need to be done to accommodate remote CSM placement. The grounding scheme for the shield is also being studied.

1.5.9.4 Chamber Service Module

Milestone	Baseline	Previous	Forecast	Status
CSM-1 Prototype	1-Sep-00	--	1-Jun-02	Delayed (See #1)

CSM-1/Octal ASD/MROD Test	1-Dec-01	--	1-Jul-02	Delayed (See #2)

Note #1 The scope of the CSM-1 has changed to a simpler, more robust design. As a result the completion date of the first prototype has moved to spring 02. Work on the design for this more ambitious design is progressing.

Note #2 Testing will follow CSM-1 prototype completion and will use already tested production mezz boards with AMT-2 and the octal ASD.

1.5.11 CSC Electronics

1.5.11.1 ASM1 Boards

1.5.11.1.1 Design

Milestone	Baseline	Previous	Forecast	Status
Preamp/Shaper Final Design Review	2-Oct-01	--	1-Dec-01	Delayed (See #1)
System Critical Design Review	2-Oct-01	--	1-Dec-01	Delayed (See #2)

Note #1 Delayed to allow us to verify design modifications to preamp/shaper for yield enhancement, reduced crosstalk, and improved overload recovery. Work along these lines continued in Oct.

Note #2 Delayed to allow us to verify design modifications to preamp/shaper for yield enhancement, reduced crosstalk, and improved overload recovery. Continued in Sept.

1.5.11.5 ROD's

1.5.11.5.2 ROD Prototype

Milestone	Baseline	Previous	Forecast	Status
RODs Final Design Review	4-Mar-02	--	4-Mar-02	On Schedule

David Stoker (University of California Irvine)

During October, we continued incremental assembly and testing of the ROD motherboard. We received a five-slot VME backplane to help facilitate testing of the ROD prototype, and successfully powered the ROD motherboard from this backplane. We received and installed BGA (ball grid array) rework equipment to aid ROD assembly, and completed an operator training session. We investigated multichannel optoelectronics for the CSC transition module, which interfaces the ROD with the on-

detector electronics and also contains the Readout Link. The multichannel transmitters and receivers require substantially less power, board area, and back panel area than other anticipated solutions.

1.5.11.7 Software

1.5.11.7.1 Software Design

Milestone	Baseline	Previous	Forecast	Status
S/W Conceptual Design Review	2-May-01	--	15-Jan-02	Delayed (See #1)

Note #1 Development of code external to ROD and documentation not ready for review.

David Stoker (University of California Irvine)

During October, we continued coding of the SPU (Sparsifier Processing Unit) C and assembly code. Histogramming capabilities were added to the RPU (Rejection Processing Unit) code. We also began developing software for communicating between a PC and the ROD motherboard via VME. This software will, for example, be used to program the ROD's flash memory with FPGA configuration streams and HPU executable code.

1.5.12 Global Alignment System — Jim Bensinger (Brandeis University)

Although we lost access to the H8 area because the beam was on, some progress was made on assembly and survey of the installation. The EOL chamber was dismounted and the mounts correctly surveyed into place. Some serious interference problems with the layout of the EO BCAMs in H8 were discovered.

Work continued on the Big Wheel with Ken Wynn spending a week at CERN working with the Snezinsk group and CERN personnel on the Design. Work on including the CSCs in the global alignment system included going to BNL for a meeting with the CSC group and developing a design to include these items.

We have also made engineering change requests regarding the modifications to the extreme feet of the ATLAS detector. We are also working on the version P of the parameter book.

1.5.12.1 Global Design

1.5.12.1.1 Alignment Bars

Milestone	Baseline	Previous	Forecast	Status
Alignment Bar Design Complete	30-Mar-01	--	30-Mar-02	Delayed (See #1)

Note #1 Design for H8 is complete and there is no work on this item at this time. This design will be reviewed following analysis of H8 results. Final design will take place at that time.

Jim Bensinger (Brandeis University)

We have evaluated the change to an 85 mm alignment bar. This appears possible for the long bars. The length of the EM alignment bars was modified to account for the wheel movements.

1.5.12.1.2 Proximity Monitors — Jim Bensinger (Brandeis University)

A complete set of proximity cameras for H8 was made and shipped to CERN. Bar masks for H8 were designed and submitted to the shop.

1.5.12.1.3 Multi-Point System (BCAM)

Milestone	Baseline	Previous	Forecast	Status
BCAM Design Complete	31-Dec-01	--	31-Dec-01	On Schedule

Jim Bensinger (Brandeis University)

Two BCAMs were sent to CERN for evaluation. Studies at CERN, Seattle, and Brandeis about the behavior on heating show unexpected motions of the light sources. This is not a problem for ATLAS since it happens during heating and ATLAS running is expected to have a stable thermal environment, but we continue the study to make sure there are not additional problems. Electronics boards for 100 BCAMs have been ordered; the mechanical parts exist.

1.5.12.1.4 System Design — Jim Bensinger (Brandeis University)

We have taken on the responsibility, along with the CERN of updating the parameter book for the endcap system. We have work with the Snezinsk group to insure there are no interference's with either MDT chambers or the alignment components in the big wheel. We have also worked on integration of the endcap MDT system, including placement of B-field sensors (current parameter book location interfere with gas distribution systems), location of survey targets.

1.5.12.1.5 DAQ

Milestone	Baseline	Previous	Forecast	Status
DAQ Design Complete	28-Sep-01	--	30-Mar-02	Delayed (See #1)

Note #1 The H8 version basic design is complete. This design will be reevaluated following analysis of H8 data and, if needed, will be revised at that time.

Jim Bensinger (Brandeis University)

Fixed the problem with the multiplexers and submitted new layout to vendor for more boards. Wrote a report on the BCAM light source. We have ordered assembled header and peripheral header for 100 BCAMs.

A good deal of time was spent responding to H8 problems including tracking down faulty cables and headers, and understanding thermal behavior of the BCAMs.

1.5.12.2 Operational Test Stands

1.5.12.2.3 H8 DATCHA

Milestone	Baseline	Previous	Forecast	Status
H8 Operational	24-Nov-00	--	15-Nov-01	Delayed (See #1)

Note #1 The area will be unavailable for mounting devices for much of October because the beam will be on. Most components are expected to arrive in October and mounted early November.

Jim Bensinger (Brandeis University)

Continued work on and debugging H8. We made the struts for the EI and EM chambers (Seattle will make them for ATLAS but we had to make them for H8). Designed transfer plates to correct for the incorrect mounting positions of the EM octant as designed by Snezinsk. Provided coordinates for surveyors to install chamber mounts. There are problems of lines of sight for the EO frames; we are working on these problems.

1.5.12.3 Global System Production

Milestone	Baseline	Previous	Forecast	Status
Align Bar/Prox Monitors PRR	3-Jan-01	--	31-Mar-02	Delayed (See #1)
Critical System Design Review	3-Jan-01	--	31-Mar-02	Delayed (See #2)

Note #1-2 Not yet scheduled but will follow analysis of H8 results.

Jim Bensinger (Brandeis University)

The part of system production that has begun is that relating to the production of MDT chambers, the inplane system and the camera mounts and mask mounts for the proximity monitors that go on the chambers.

1.5.12.3.1 Alignment Bars

Milestone	Baseline	Previous	Forecast	Status
Bar Production 10% Complete	1-Oct-01	--	1-Jun-02	Delayed (See #1)

Note #1 This is no longer a US responsibility and will be done at Freiburg. Bar production will not begin until after analysis of H8 results.

1.5.12.3.2 Proximity Monitors

Milestone	Baseline	Previous	Forecast	Status
Prox. Production 10% Complete	1-Jan-02	1-Jan-02	1-Jul-02	Delayed (See #1)

Note #1 For final design of the proximity monitors, we must know the position of all components to within 10 mm. Since the layout of ATLAS is not yet final, we are holding the start of production until the layout is final. Production can be completed quickly so this will have no overall schedule impact.

Jim Bensinger (Brandeis University)

We have delivered all the mask and camera mounts for the second round of production to the US production sites.

1.5.12.3.3 Multi-Point System (BCAM)

Milestone	Baseline	Previous	Forecast	Status
BCAM Production Begins	1-Jan-02	1-Jan-02	1-Jul-02	Delayed (See #1)

Note #1 Final BCAM production will not begin until after the PRR. This has not yet been scheduled.

1.5.12.4 MDT Inplane Monitors

1.5.12.4.1 Common Items

Milestone	Baseline	Previous	Forecast	Status
Common Items 25% Complete	1-Jan-02	--	1-Jan-02	On Schedule

Jim Bensinger (Brandeis University)

Almost all of the common parts for the approved MDT chamber production now exists at Brandeis or are mounted on produced chambers.

1.5.12.4.6 EIS2 (Boston)

Milestone	Baseline	Previous	Forecast	Status
Ship to Site	23-Oct-01	--	1-Feb-02	Delayed (See #1)

Note #1 Changes in MDT production schedule has moved this chamber to the third round of production. Since this is a special chamber, confirmation of the inplane design will await completion of the design of the chamber.

Jim Bensinger (Brandeis University)

Design has begun for chamber specific parts, all other exits. Lenses exist and have been measured.

1.5.12.4.13 EML3 (Michigan)

Milestone	Baseline	Previous	Forecast	Status

Ship to Site	10-Dec-01	--	10-Dec-01	On Schedule

Jim Bensinger (Brandeis University)

Design has begun for chamber specific parts, all other exits. Lenses exist and have been measured.

1.5.12.4.18 EMS3 (Seattle)

Milestone	Baseline	Previous	Forecast	Status
Ship to Site	7-Sep-01	1-Apr-02	1-Jan-02	Delayed (See #1)

Note #1 This chamber is not scheduled to be built until the third round of MDT production. Since this is a special chamber, confirmation of the inplane design will await completion of the design of the chamber.

Jim Bensinger (Brandeis University)

This is a special chamber with a cutout. This requires one additional RASNIK line and an additional cross plate. The design for the chamber modification is being done at Brandeis in conjunction with Seattle and the inplane system is part of that design effort. This is well underway.

1.6 TRIGGER

Milestones with changed forecast dates:

1.6 Subsystem Manager's Summary

Milestone	Baseline	Previous	Forecast	Status
Start Installation & Commissioning	5-Mar-02	5-Mar-02	5-Mar-03	Delayed (See #1)

Note #1 Production will proceed after design and consistent with the current ATLAS TDAQ schedule.

1.6.1.2.4 SRB Prototype Travel

Milestone	Baseline	Previous	Forecast	Status
Prototype SRB Assy Compl	30-Sep-01	30-Nov-01	30-Mar-02	Delayed (See #1)

Note #1 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. Since the current prototype SRB may be adequate for early use in the experiment, the level 1 group has suggested that the system undergo more formal design review and documentation prior to production. The current 12U board is adequate for phase 2 tests (if a hardware implementation is regarded as important - this is not yet clear). Tests of the new SRB with level 1 components will not proceed until spring or summer in '02 so this does not delay anything significantly.

1.6.3.2 SCT Protos

Milestone	Baseline	Previous	Forecast	Status

Prototype SCT Assy Compl	30-Sep-01	31-Oct-01	30-Nov-01	Delayed (See #1)

Note #1 This prototype completion was originally delayed to the end of October in order to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is presently expected to be completed at the end of November.

Milestone	**Baseline**	**Previous**	**Forecast**	**Status**
LVL2 Trigger Prototype Complete	30-Sep-01	--	30-Nov-01	Delayed (See #1)
LVL2 Trigger Design Complete	31-Dec-01	--	31-Dec-02	Delayed (See #2)
Start Production	8-Jan-02	--	8-Jan-03	Delayed (See #3)
Start Installation & Commissioning	5-Mar-02	5-Mar-02	5-Mar-03	Delayed (See #4)

Note #1 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of November.

Note #2 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The TDR is scheduled for the end of Dec. '02. This is the earliest date possible for a complete design.

Note #3 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The production will start after design is complete.

Note #4 Production will proceed after design and consistent with the current ATLAS TDAQ schedule.

1.6.1 LVL2 SRB

1.6.1.2 SRB Protos

1.6.1.2.1 SRB Protos EDIA — Robert Blair (Argonne National Lab.)

At ATLAS week during discussions with the Level 1 group the decision to subject the Supervisor RoI Builder hardware to the level 1 design process was made. This means that the actual board design needs to be prefaced by a set of design documents and a formal design review. It was felt that the next version of the RoI builder was close enough to a final version that it should be done in such a way that it might be used for initial running. A more formal design process would slow things down a bit, but since the labor needed for a next generation test with level 1 components would be occupied through the first half of '02 on the Heidelberg slice test this would not introduce any delay. The phase 2 program for level 2 has no clear need for a hardware RoI builder and even if tests with one are considered important the 12U one will suffice for this.

The link source cards (S-link mezzanine cards) for use on the RoI builder are being considered as a good candidate for Readout Buffer on ROD tests. This card includes a 512k word buffer and an FPGA on the ROD driver card and can be configured to act as a primitive ROB (or ROBin). Since the card uses gigabit ethernet it could be connected directly to a network switch and send data to a requestor. Mannheim and CERN would like to get early versions of this card to allow them to program the FPGA for this type of

use. ANL will provide cards once the point-to-point functionality required for the RoIB and the hardware itself is sufficiently checked out.

Bernard Pope (Michigan State University)

Abolins, Hauser and Ermoline attended the ATLAS week at CERN (October 15-19). Two meetings were held with the Liquid Argon ROD designers; information is on the ROD Working Group web page (http://atlasinfo.cern.ch/Atlas/GROUPS/DAQTRIG/DIG/ROD/). Also a LVL1-Dataflow meeting took place during ATLAS week. It was agreed that ROIB documentation should be prepared for the Preliminary Design Review. Abolins participated in a meeting on Modeling and contributed to discussions concerning LVL1-LVL2 interface activities. Dataflow integration activities for the coming months were also discussed.

1.6.1.2.4 SRB Prototype Travel

Milestone	Baseline	Previous	Forecast	Status
Prototype SRB Assy Compl	30-Sep-01	30-Nov-01	30-Mar-02	Delayed (See #1)

Note #1 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. Since the current prototype SRB may be adequate for early use in the experiment, the level 1 group has suggested that the system undergo more formal design review and documentation prior to production. The current 12U board is adequate for phase 2 tests (if a hardware implementation is regarded as important - this is not yet clear). Tests of the new SRB with level 1 components will not proceed until spring or summer in '02 so this does not delay anything significantly.

1.6.2 LVL2 Calorimeter Trg

1.6.2.1 Calo Design

1.6.2.1.1 Calo Design EDIA — Saul Gonzalez (University of Wisconsin)

The ZEBRA data input for the calorimeter algorithms has been successfully tested using data samples at low and high luminosity.

1.6.2.2 Calo Protos

Milestone	Baseline	Previous	Forecast	Status
Prototype Calo Assy Compl	30-Sep-01	--	30-Nov-01	Delayed (See #1)

Note #1 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of November.

1.6.3 LVL2 SCT Trg

1.6.3.1 SCT Design

1.6.3.1.1 SCT Design EDIA **A.J. Lankford (University of Calif. at Irvine)**

Specification of the ROD/ROB interface continued in October. The ATLAS ROD Working Group Readout Link Task Force focused on evaluation of costs of alternative implementations for the physical link was initiated. Implementations involving different numbers of fibers per Readout Link and implementation with electrical connections were examined. Issues concerning length of the Readout Link, and hence relative locations of ROD and ROB, and patch panels were considered.

Study of the system implications of a network-based Readout Subsystem (ROS) continued. Consideration of mounting the ROBs on mezzanines on the ROBS continued in this context. Studies were extended from the ROS working group to include the systems on either side of the ROS, including the ROD working group of the Detector Interface Group and the Data Collection working group. This concept was discussed during the Dataflow Session of the October ATLAS Week.

Saul Gonzalez (University of Wisconsin)

There is no ongoing algorithm development work. The bulk of the effort now is in framework development.

1.6.3.1.4 SCT Design Travel

Milestone	Baseline	Previous	Forecast	Status
SCT for Integ Study Compl	30-Sep-01	--	30-Nov-01	Delayed (See #1)

Note #1 This prototype preliminary exploitation has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of November.

1.6.3.2 SCT Protos

Milestone	Baseline	Previous	Forecast	Status
Prototype SCT Assy Compl	30-Sep-01	31-Oct-01	30-Nov-01	Delayed (See #1)

Note #1 This prototype completion was originally delayed to the end of October in order to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is presently expected to be completed at the end of November.

1.6.4 Architecture & LVL2 Global Trigger

1.6.4.1 Arch. Design

1.6.4.1.1 Arch. Design EDIA — A.J. Lankford (University of Calif. at Irvine)

Work continued with TDAQ system leaders on project planning for the development and prototyping period preceding the HLT/DAQ/DCS TDR. Detailed WBS and schedule were completed for all the HLT/DAQ systems. A summary WBS and schedule were also completed for Technical Coordination. These planning documents only cover the period before the HLT/DAQ/DCS TDR, which will be submitted at the end of 2002. Planning and preparation for the TDAQ Activity/System Status Overview (ASSO) was completed. The ASSO was held during TDAQ Week.

Work continued on developing "strawman" dataflow architectures to serve as a starting point for performance studies in the integrated prototyping. Investigation of event fragment sizes, in order to establish overall data bandwidth requirements was initiated. Definition of test bed configurations for performance tests of the dataflow architectures progressed, but is tied to the definition of the architectures to be tested. Testbed configurations for functionality tests of the Phase 2A integrated prototype were defined.

Bernard Pope (Michigan State University)

Work included preparations for various talks and sessions during the ATLAS week. The TCP implementation of the Datacollection message passing was finished after bugs were found in initial testing. A release procedure was implemented for the Datacollection software and first test releases were produced. A first draft of a document on the "ROB on ROD" issue was written. This will be presented during the November TDAQ week in NIKHEF.

1.6.4.1.4 Arch. Design Travel

Milestone	Baseline	Previous	Forecast	Status
Prototype Project Assy Compl	30-Sep-01	--	30-Nov-01	Delayed (See #1)

Note #1 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of November.

1.6.4.2 Global Production

1.6.4.2.1 Global Prod Eqmt — Saul Gonzalez (University of Wisconsin)

W.Wiedenmann has continued his benchmarking studies with the Athena framework. During October, the crucial event model component of the framework ("RD Event") was instrumented. Measurements with jet events at high luminosity showed that the event model consumes ~30% of the total execution time of the Event Filter. This result underscores the importance of present efforts to coordinate a sensible event model with the offline community.

Other recent results, obtained in collaboration with the Barcelona EF group, include detailed measurements of the EF byte-stream converter. This converter, an essential component of the EF, transforms the byte-stream (concatenated event fragments) generated by the event builder into offline objects. These objects are organized according to the RD event model. Results obtained in October indicate that this conversion takes ~ 500 ms per event using the Lund release of the offline software. These results and future plans from the Athena suitability studies were presented at an HLT Dataflow meeting in October.